ZQ2B SOLE UMA SYSTEM DIAGRAM

AMD Smarter Choice
Danube Platform
(Main Stream)

VER : 1A

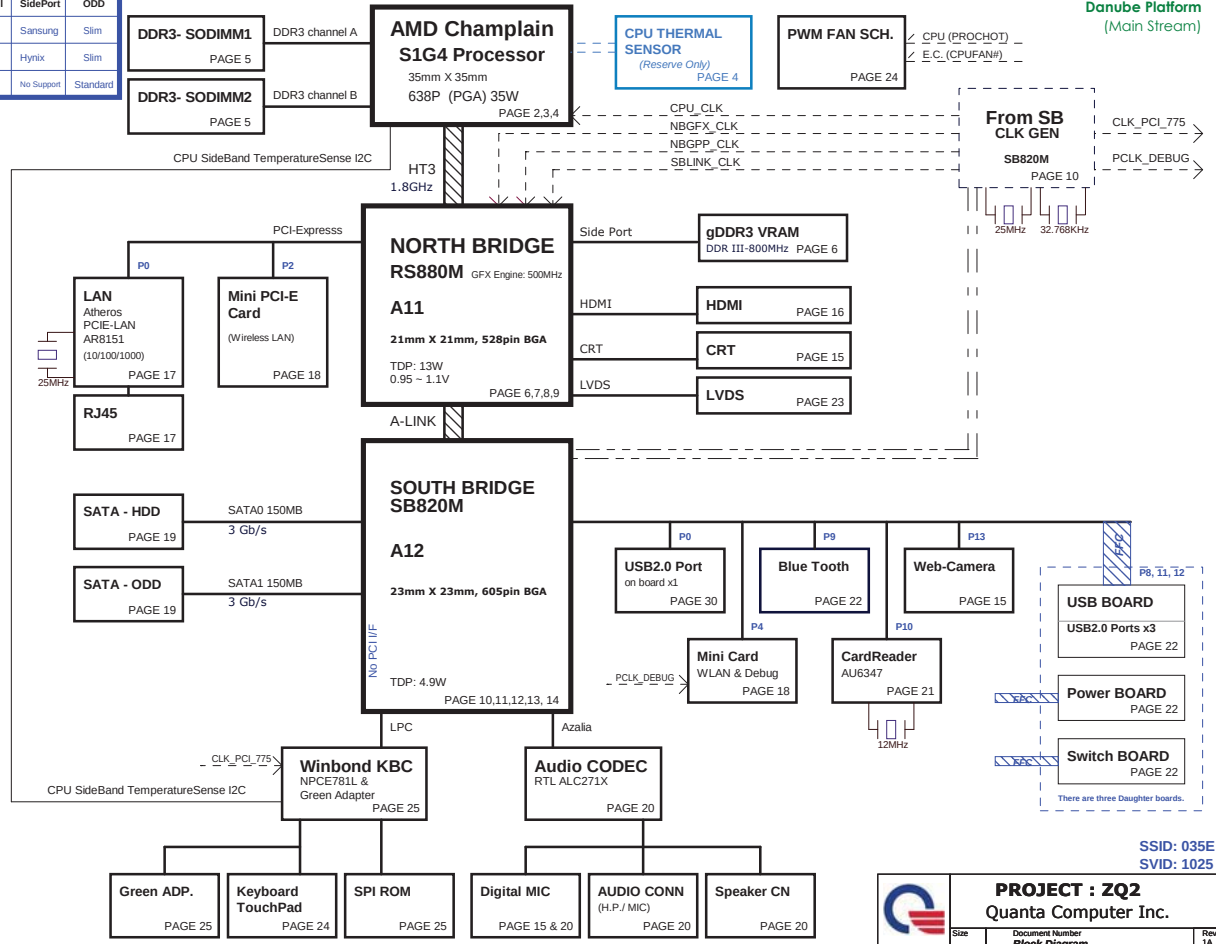
BOM P/N	Description	Model	SidePort	ODD
31ZQ2MB00A0	ZQ2B 6L JM MB (W/GRN,SAM,W/O CPU)ASSY	JM	Sansung	Slim
31ZQ2MB00E0	ZQ2B 6L JM MB (W/GRN,HYU,W/O CPU)ASSY	JM	Hynix	Slim
31ZQ2MB00H0	ZQ2B 6L JV MB (W/GRN,W/O CPU,VRAM)ASSY	JV	No Support	Standard

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

IV@ -----> iGPU
SP@ -----> Option Notice
SIDE@ -----> SidePort VRAM
GA@ ----> Green Adapter (Default stuff)

Sideport-L75,L76,R583,R392,C832,R455,R550,R502
NB A11-R105,R108
SB A12-R267,R271
JV/JM-CN16,R450,R456
EC-D8,D27
UMA-R461
VRAM-R358,R359,R360,R363,R365,R72



CHARGER (ISL88731A) PAGE 26
AMD CPU CORE (ISL6265) PAGE 28 — CPU
NB_CORE (UP6111AQDD) PAGE 30 — NB
0.9V/DDR 1.5V(RT8207) PAGE 31
SYSTEM 5V/3V (RT8206) PAGE 27
1.1V(UP6111AQDD) PAGE 29
Discharge /Thermal protec PAGE 32

SSID: 035E
SVID: 1025

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	1A

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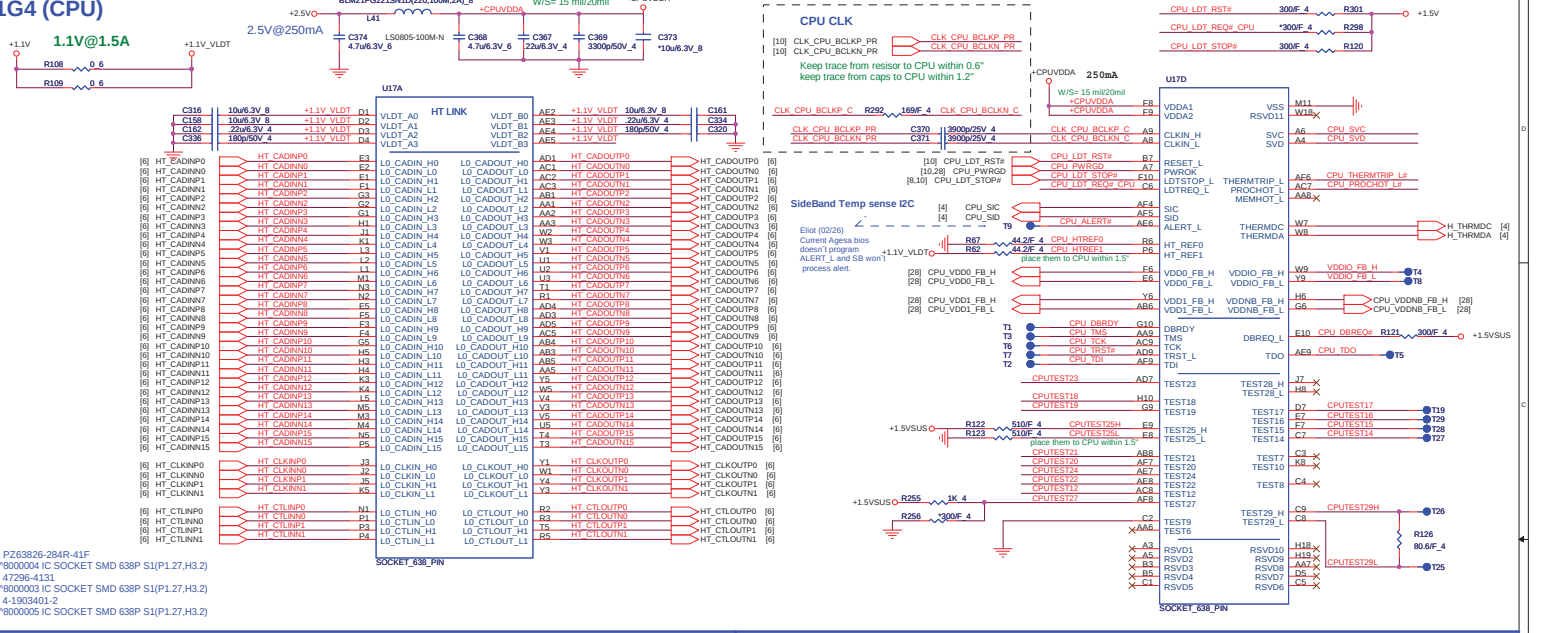
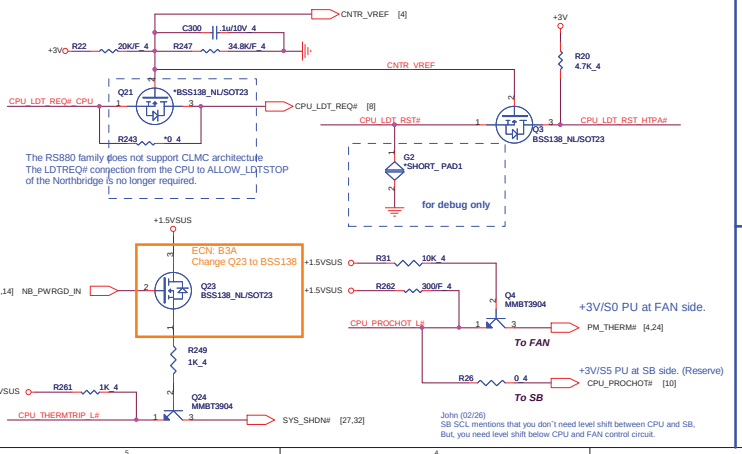
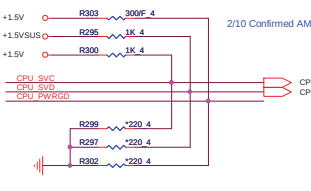
S1G4 (CPU)



FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)



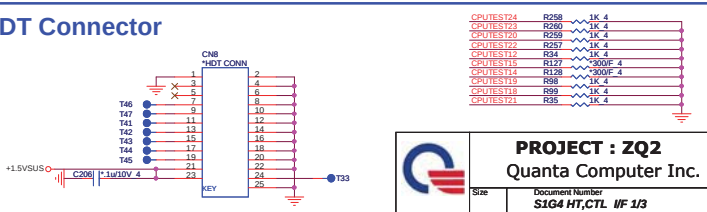
Serial VID



VFIX MODE — VID Override Circuit

SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

HDT Connector



PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	S1G4 HT,CTL I/F 1/3	1A

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35W CPU support 0.9V
45W CPU support 1.05V

VDDR=> 0.9V support 1066 / 800 DDR
VDDR= >1.05V support 1333 / 1066 / 800 DDR

VDDR=>1.75A

PLACE THEM CLOSE TO CPU WITHIN 1"

+1.5VSUS
R250 0_4
C307 10u/6.3V_8
CPU_VDDR
U17B
R253 39.2/F_4 M_ZP
R254 39.2/F_4 M_ZN
MEM:CMD/CTRL/CLK
VDDR1 VDDR2 VDDR3 VDDR4 VDDR5 VDDR6 VDDR7 VDDR8 VDDR9
MEMZP MEMZN VDDR_SENSE
CPU_VDDR
CPU_VDDR
Y10 CPU_VTT_SENSE
R37 *0_4
W17 MEMVREF_CPU
MEMVREF
+SMDDR_VREF
R33 *0_4
C31 1u/10V_4
C35 1000P/50V_4

[5] M_A_RST#
[5] M_A_ODT0
[5] M_A_ODT1
[5] M_A_CS#0
[5] M_A_CS#1
[5] M_A_CKE0
[5] M_A_CKE1
[5] M_A_CLKP1
[5] M_A_CLKN1
[5] M_A_CLKP2
[5] M_A_CKN2
[5] M_A_A[0..15]
[5] M_A_BANK0
[5] M_A_BANK1
[5] M_A_BANK2
[5] M_A_RAS#
[5] M_A_CAS#
[5] M_A_WE#

MA_RESET_L, MA0_ODT0, MA_ODT1, MA0_CS_L0, MA0_CS_L1, MA1_CS_L0, MA1_CS_L1, MA_CKE0, MA_CKE1, MA_CLK_H5, MA_CLK_L5, MA_CLK_H1, MA_CLK_L1, MA_CLK_H7, MA_CLK_L7, MA_CLK_H4, MA_CLK_L4, MA_ADD0, MA_ADD1, MA_ADD2, MA_ADD3, MA_ADD4, MA_ADD5, MA_ADD6, MA_ADD7, MA_ADD8, MA_ADD9, MA_ADD10, MA_ADD11, MA_ADD12, MA_ADD13, MA_ADD14, MA_ADD15, MA_BANK0, MA_BANK1, MA_BANK2, MA_RAS_L, MA_CAS_L, MA_WE_L

MB_RESET_L, MB0_ODT0, MB0_ODT1, MB1_ODT0, MB0_CS_L0, MB0_CS_L1, MB1_CS_L0, MB1_CS_L1, MB_CKE0, MB_CKE1, MB_CLK_H5, MB_CLK_L5, MB_CLK_H1, MB_CLK_L1, MB_CLK_H7, MB_CLK_L7, MB_CLK_H4, MB_CLK_L4, MB_ADD0, MB_ADD1, MB_ADD2, MB_ADD3, MB_ADD4, MB_ADD5, MB_ADD6, MB_ADD7, MB_ADD8, MB_ADD9, MB_ADD10, MB_ADD11, MB_ADD12, MB_ADD13, MB_ADD14, MB_ADD15, MB_BANK0, MB_BANK1, MB_BANK2, MB_RAS_L, MB_CAS_L, MB_WE_L

[5] M_B_ODT0
[5] M_B_ODT1
[5] M_B_CS#0
[5] M_B_CS#1
[5] M_B_CKE0
[5] M_B_CKE1
[5] M_B_CLKP1
[5] M_B_CLKN1
[5] M_B_CLKP2
[5] M_B_CLKN2
[5] M_B_A[0..15]
[5] M_B_BANK0
[5] M_B_BANK1
[5] M_B_BANK2
[5] M_B_RAS#
[5] M_B_CAS#
[5] M_B_WE#

SOCKET_638_PIN

Place close to socket

CPU_VDDR

C174 4.7u/6.3V_6, C34 4.7u/6.3V_6, C33 4.7u/6.3V_6, C175 4.7u/6.3V_6, C169 .22u/6.3V_4, C170 .22u/6.3V_4, C39 .22u/6.3V_4, C37 .22u/6.3V_4

C168 1000P/50V_4, C171 1000P/50V_4, C145 1000P/50V_4, C40 1000P/50V_4, C172 180p/50V_4, C38 180p/50V_4, C166 180p/50V_4, C36 180p/50V_4

Reserved for AMD suggest

+1.5VSUS
R24 1K/F_4
R25 1K/F_4
C29 *.47u/10V_4
R30 0_4
+3VPCU
C27 *.1u/10V_4
U2 *OPA343NA/3K
R28 *10_4
MEMVREF_CPU
R29 *10K_4
R23 *0_4
R27 *0_4

Processor Memory Interface

[5] M_B_DQ[0..63]
U17C
MEM:DATA
M_B_DQ0 C11 MB_DATA0 MA_DATA0 G12 M_A_DQ0
M_B_DQ1 A11 MB_DATA1 MA_DATA1 E12 M_A_DQ1
M_B_DQ2 A14 MB_DATA2 MA_DATA2 H14 M_A_DQ2
M_B_DQ3 B14 MB_DATA3 MA_DATA3 G14 M_A_DQ3
M_B_DQ4 G11 MB_DATA4 MA_DATA4 H11 M_A_DQ4
M_B_DQ5 E11 MB_DATA5 MA_DATA5 H12 M_A_DQ5
M_B_DQ6 D12 MB_DATA6 MA_DATA6 C13 M_A_DQ6
M_B_DQ7 A13 MB_DATA7 MA_DATA7 E13 M_A_DQ7
M_B_DQ8 A15 MB_DATA8 MA_DATA8 H15 M_A_DQ8
M_B_DQ9 A16 MB_DATA9 MA_DATA9 E15 M_A_DQ9
M_B_DQ10 A19 MB_DATA10 MA_DATA10 E17 M_A_DQ10
M_B_DQ11 A20 MB_DATA11 MA_DATA11 H17 M_A_DQ11
M_B_DQ12 C14 MB_DATA12 MA_DATA12 E14 M_A_DQ12
M_B_DQ13 D14 MB_DATA13 MA_DATA13 F14 M_A_DQ13
M_B_DQ14 C18 MB_DATA14 MA_DATA14 C17 M_A_DQ14
M_B_DQ15 D18 MB_DATA15 MA_DATA15 G17 M_A_DQ15
M_B_DQ16 D20 MB_DATA16 MA_DATA16 G18 M_A_DQ16
M_B_DQ17 A21 MB_DATA17 MA_DATA17 C19 M_A_DQ17
M_B_DQ18 D24 MB_DATA18 MA_DATA18 D22 M_A_DQ18
M_B_DQ19 C25 MB_DATA19 MA_DATA19 E20 M_A_DQ19
M_B_DQ20 B20 MB_DATA20 MA_DATA20 E18 M_A_DQ20
M_B_DQ21 C20 MB_DATA21 MA_DATA21 F18 M_A_DQ21
M_B_DQ22 B24 MB_DATA22 MA_DATA22 B22 M_A_DQ22
M_B_DQ23 C24 MB_DATA23 MA_DATA23 C23 M_A_DQ23
M_B_DQ24 E23 MB_DATA24 MA_DATA24 F20 M_A_DQ24
M_B_DQ25 E24 MB_DATA25 MA_DATA25 E22 M_A_DQ25
M_B_DQ26 G25 MB_DATA26 MA_DATA26 H24 M_A_DQ26
M_B_DQ27 G26 MB_DATA27 MA_DATA27 J19 M_A_DQ27
M_B_DQ28 C26 MB_DATA28 MA_DATA28 E21 M_A_DQ28
M_B_DQ29 D26 MB_DATA29 MA_DATA29 E22 M_A_DQ29
M_B_DQ30 G23 MB_DATA30 MA_DATA30 H20 M_A_DQ30
M_B_DQ31 G24 MB_DATA31 MA_DATA31 H22 M_A_DQ31
M_B_DQ32 AA24 MB_DATA32 MA_DATA32 Y24 M_A_DQ32
M_B_DQ33 AA23 MB_DATA33 MA_DATA33 AB24 M_A_DQ33
M_B_DQ34 AD24 MB_DATA34 MA_DATA34 AB22 M_A_DQ34
M_B_DQ35 AE24 MB_DATA35 MA_DATA35 AA21 M_A_DQ35
M_B_DQ36 AA26 MB_DATA36 MA_DATA36 W22 M_A_DQ36
M_B_DQ37 AA25 MB_DATA37 MA_DATA37 W21 M_A_DQ37
M_B_DQ38 AD26 MB_DATA38 MA_DATA38 Y22 M_A_DQ38
M_B_DQ39 AE25 MB_DATA39 MA_DATA39 AA22 M_A_DQ39
M_B_DQ40 AC22 MB_DATA40 MA_DATA40 Y20 M_A_DQ40
M_B_DQ41 AD22 MB_DATA41 MA_DATA41 AA20 M_A_DQ41
M_B_DQ42 AE20 MB_DATA42 MA_DATA42 AA18 M_A_DQ42
M_B_DQ43 AD20 MB_DATA43 MA_DATA43 AB18 M_A_DQ43
M_B_DQ44 AF24 MB_DATA44 MA_DATA44 AB21 M_A_DQ44
M_B_DQ45 AF23 MB_DATA45 MA_DATA45 AD21 M_A_DQ45
M_B_DQ46 AC20 MB_DATA46 MA_DATA46 AD19 M_A_DQ46
M_B_DQ47 AD20 MB_DATA47 MA_DATA47 Y18 M_A_DQ47
M_B_DQ48 AE18 MB_DATA48 MA_DATA48 AD17 M_A_DQ48
M_B_DQ49 AE18 MB_DATA49 MA_DATA49 W16 M_A_DQ49
M_B_DQ50 AC14 MB_DATA50 MA_DATA50 W14 M_A_DQ50
M_B_DQ51 AD14 MB_DATA51 MA_DATA51 Y14 M_A_DQ51
M_B_DQ52 AE19 MB_DATA52 MA_DATA52 Y17 M_A_DQ52
M_B_DQ53 AC18 MB_DATA53 MA_DATA53 AB17 M_A_DQ53
M_B_DQ54 AF16 MB_DATA54 MA_DATA54 AB15 M_A_DQ54
M_B_DQ55 AE15 MB_DATA55 MA_DATA55 AD15 M_A_DQ55
M_B_DQ56 AE13 MB_DATA56 MA_DATA56 AB13 M_A_DQ56
M_B_DQ57 AC12 MB_DATA57 MA_DATA57 AD13 M_A_DQ57
M_B_DQ58 AB11 MB_DATA58 MA_DATA58 Y12 M_A_DQ58
M_B_DQ59 Y11 MB_DATA59 MA_DATA59 W11 M_A_DQ59
M_B_DQ60 AE14 MB_DATA60 MA_DATA60 AB14 M_A_DQ60
M_B_DQ61 AF14 MB_DATA61 MA_DATA61 AA14 M_A_DQ61
M_B_DQ62 AE11 MB_DATA62 MA_DATA62 AB12 M_A_DQ62
M_B_DQ63 AD11 MB_DATA63 MA_DATA63 AA12 M_A_DQ63

[5] M_B_DM[0..7]
M_B_DM0 A12 MB_DM0 MA_DM0 E12 M_A_DM0
M_B_DM1 B16 MB_DM1 MA_DM1 C15 M_A_DM1
M_B_DM2 A22 MB_DM2 MA_DM2 E19 M_A_DM2
M_B_DM3 E25 MB_DM3 MA_DM3 F24 M_A_DM3
M_B_DM4 AB26 MB_DM4 MA_DM4 AC24 M_A_DM4
M_B_DM5 AE22 MB_DM5 MA_DM5 Y19 M_A_DM5
M_B_DM6 AC16 MB_DM6 MA_DM6 AB16 M_A_DM6
M_B_DM7 AD12 MB_DM7 MA_DM7 Y13 M_A_DM7

[5] M_A_DQ[0..63] [5]
[5] M_A_DM[0..7] [5]

[5] M_B_DQSP0 C12 MB_DQS_H0 MA_DQS_H0 G13 M_A_DQSP0 [5]
[5] M_B_DQSN0 B12 MB_DQS_L0 MA_DQS_L0 H13 M_A_DQSN0 [5]
[5] M_B_DQSP1 D16 MB_DQS_H1 MA_DQS_H1 G16 M_A_DQSP1 [5]
[5] M_B_DQSN1 C16 MB_DQS_L1 MA_DQS_L1 G15 M_A_DQSN1 [5]
[5] M_B_DQSP2 A24 MB_DQS_H2 MA_DQS_H2 C22 M_A_DQSP2 [5]
[5] M_B_DQSN2 A23 MB_DQS_L2 MA_DQS_L2 C21 M_A_DQSN2 [5]
[5] M_B_DQSP3 F26 MB_DQS_H3 MA_DQS_H3 G22 M_A_DQSP3 [5]
[5] M_B_DQSN3 E26 MB_DQS_L3 MA_DQS_L3 G21 M_A_DQSN3 [5]
[5] M_B_DQSP4 AC25 MB_DQS_H4 MA_DQS_H4 AD23 M_A_DQSP4 [5]
[5] M_B_DQSN4 AC26 MB_DQS_L4 MA_DQS_L4 AC23 M_A_DQSN4 [5]
[5] M_B_DQSP5 AF21 MB_DQS_H5 MA_DQS_H5 AB19 M_A_DQSP5 [5]
[5] M_B_DQSN5 AF22 MB_DQS_L5 MA_DQS_L5 AB20 M_A_DQSN5 [5]
[5] M_B_DQSP6 AE16 MB_DQS_H6 MA_DQS_H6 Y15 M_A_DQSP6 [5]
[5] M_B_DQSN6 AD16 MB_DQS_L6 MA_DQS_L6 W15 M_A_DQSN6 [5]
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[5] M_B_DQSN7 AE12 MB_DQS_L7 MA_DQS_L7 W13 M_A_DQSN7 [5]

SOCKET_638_PIN

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	S1G4 DDRIII MEMORY I/F 2/3	1A

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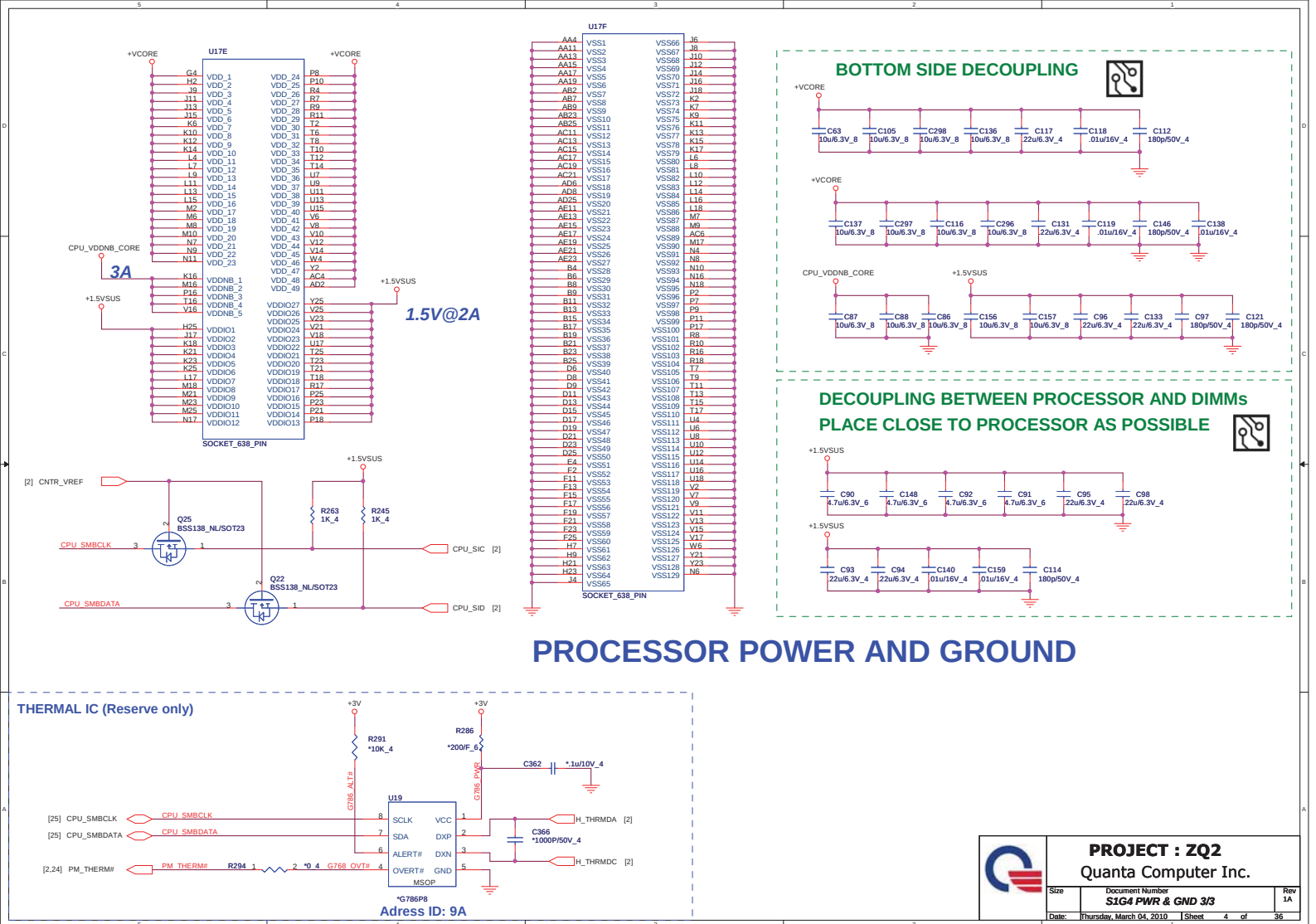
U17E
SOCKET_638_PIN
+VCORE
CPU_VDDNB_CORE
3A
+1.5VSUS
1.5V@2A
U17F
SOCKET_638_PIN
BOTTOM SIDE DECOUPLING
C63 10u/6.3V_8
C105 10u/6.3V_8
C298 10u/6.3V_8
C136 10u/6.3V_8
C117 22u/6.3V_4
C118 .01u/16V_4
C112 180p/50V_4
C137 10u/6.3V_8
C297 10u/6.3V_8
C116 10u/6.3V_8
C296 10u/6.3V_8
C131 22u/6.3V_4
C119 .01u/16V_4
C146 180p/50V_4
C138 .01u/16V_4
C87 10u/6.3V_8
C88 10u/6.3V_8
C86 10u/6.3V_8
C156 10u/6.3V_8
C157 10u/6.3V_8
C96 22u/6.3V_4
C133 22u/6.3V_4
C97 180p/50V_4
C121 180p/50V_4
DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE
C90 4.7u/6.3V_6
C148 4.7u/6.3V_6
C92 4.7u/6.3V_6
C91 4.7u/6.3V_6
C95 22u/6.3V_4
C98 22u/6.3V_4
C93 22u/6.3V_4
C94 22u/6.3V_4
C140 .01u/16V_4
C159 .01u/16V_4
C114 180p/50V_4
[2] CNTR_VREF
Q25 BSS138_NL/SOT23
Q22 BSS138_NL/SOT23
R263 1K_4
R245 1K_4
CPU_SMBCLK
CPU_SMBDATA
CPU_SIC [2]
CPU_SID [2]
PROCESSOR POWER AND GROUND
THERMAL IC (Reserve only)
+3V
R291 *10K_4
R286 *200/F_6
C362 *.1u/10V_4
G786_ALT#
G786_PWR
U19
SCLK
SDA
ALERT#
OVERT#
VCC
DXP
DXN
GND
MSOP
*G786P8
[25] CPU_SMBCLK
[25] CPU_SMBDATA
[2,24] PM_THERM#
PM_THERM#
R294 *0_4
G768_OVT#
H_THRMDA [2]
H_THRMDC [2]
C366 *1000P/50V_4
Adress ID: 9A
PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number
S1G4 PWR & GND 3/3
Rev 1A
Date: Thursday, March 04, 2010
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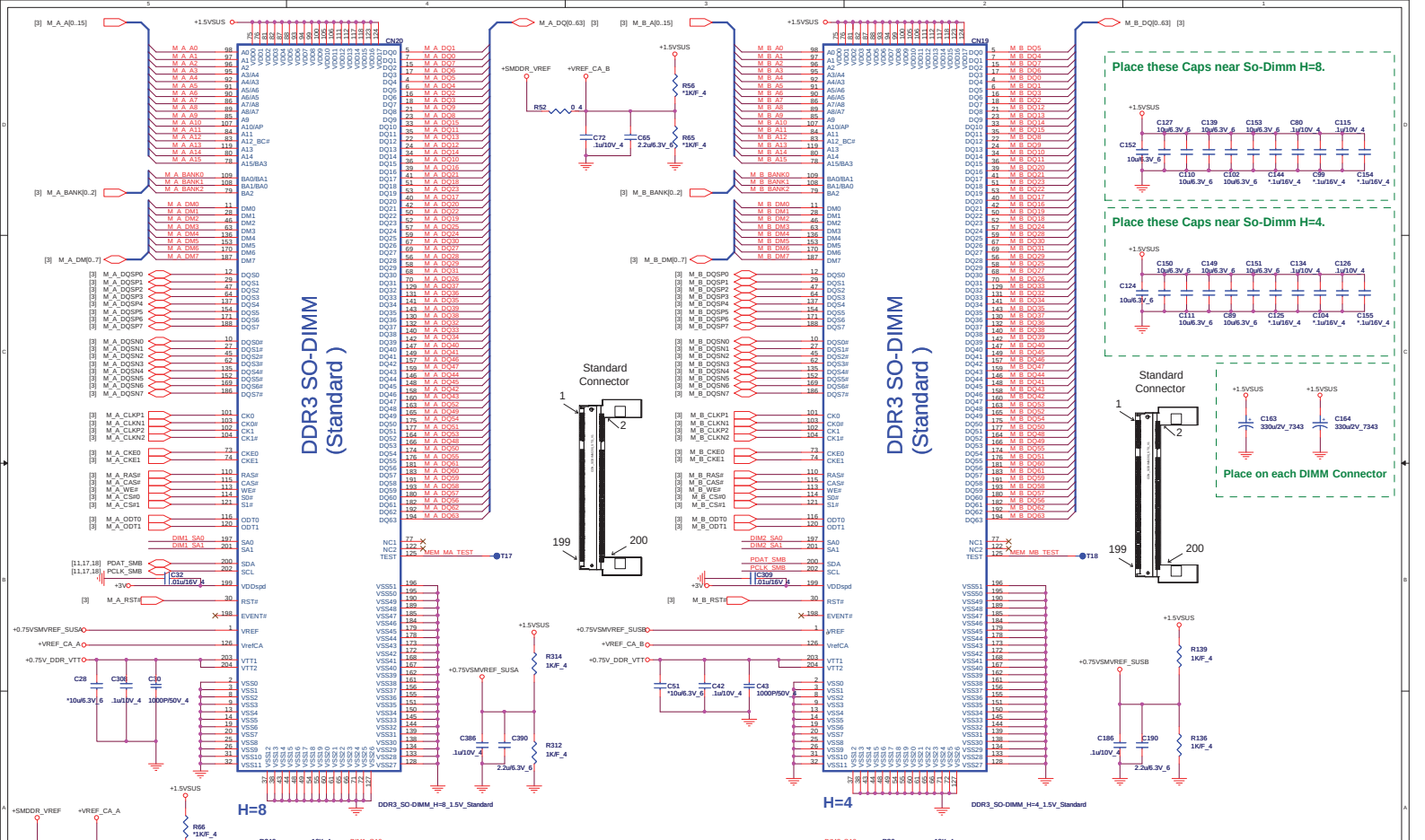
DDR3 SO-DIMM (Standard)
CN20
CN19
H=8
H=4
DDR3_SO-DIMM_H=8_1.5V_Standard
DDR3_SO-DIMM_H=4_1.5V_Standard
Standard Connector
Place these Caps near So-Dimm H=8.
Place these Caps near So-Dimm H=4.
Place on each DIMM Connector
SMbus address A0
SMbus address A2
PROJECT : ZQ2
Quanta Computer Inc.
DDR2 SODIMMS: A/B CHANNEL
Size
Document Number
Rev 1A
Date: Thursday, March 04, 2010
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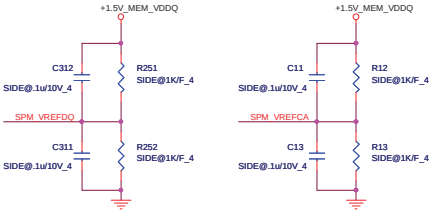
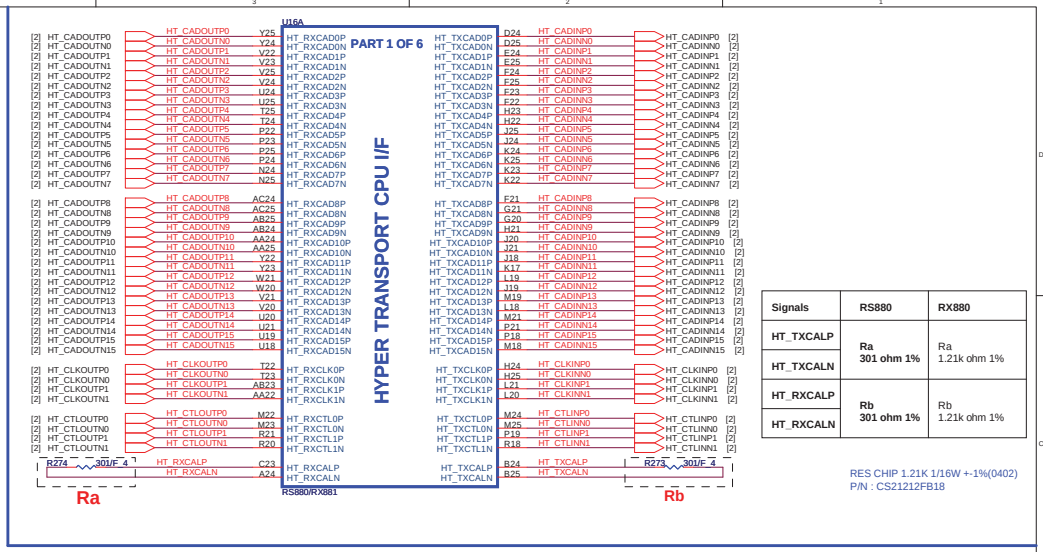
SIDE PORT

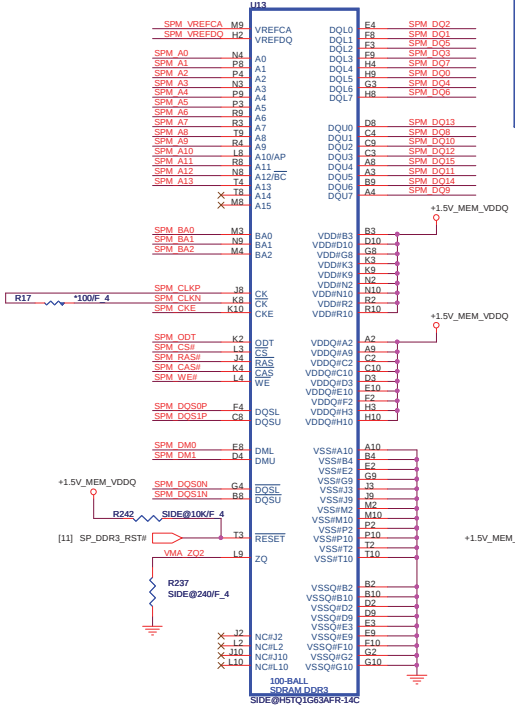


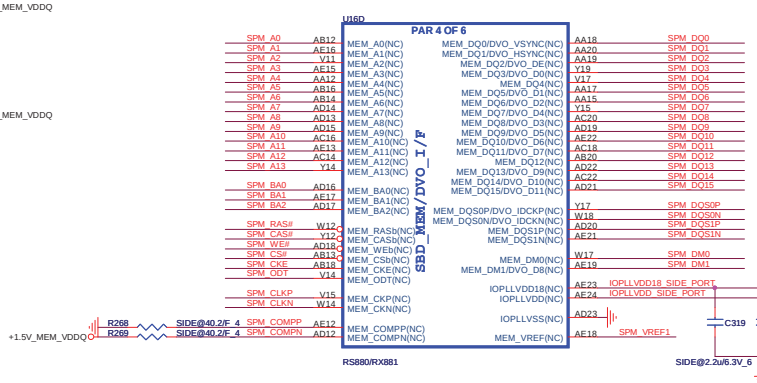


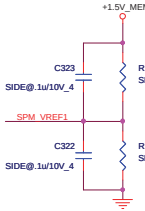
Signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

This block is for Side-Port only







IOPLLVDD18 - memory PLL
not applicable to RX881

L37 SP@BLM18PG221SN1D(220_1.4A)_6 +1.8V 15mA
L38 SP@BLM18PG221SN1D(220_1.4A)_6 +1.1V 26mA

0ohm size 0603 CS00003J951
size 0402 CS00002JB38
1K ohm CS21002FB24
Bead CX8PG221003

	W/I SP	W/O SP
R266	1K	0
L37	Bead	0
L38	Bead	0

40 mil~50 mil

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	RS880M-HT LINK I/F 1/4	1A
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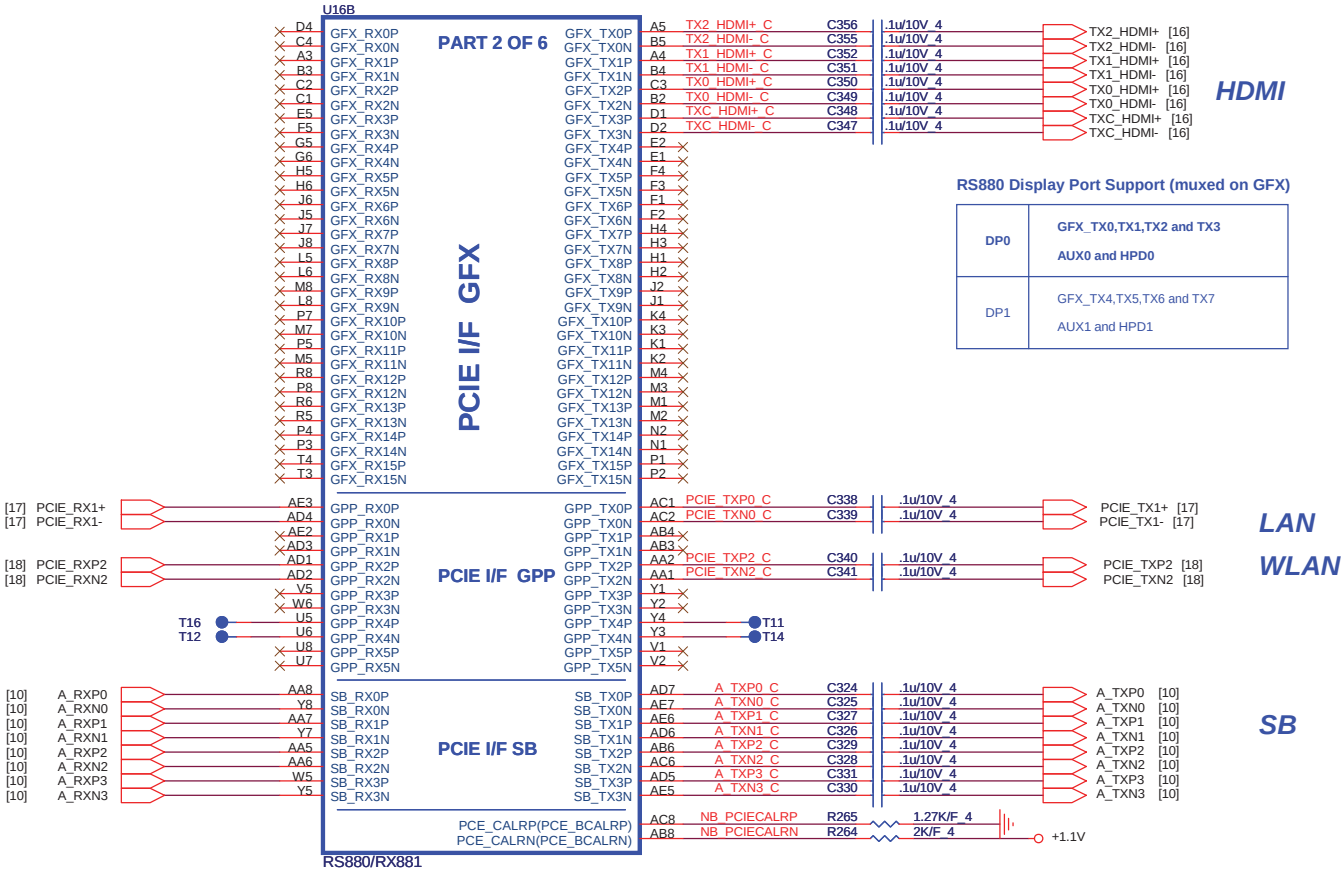

RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

Size	Document Number		Rev
	RS880M-PCIE I/F 2/4		1A
Date:	Thursday, March 04, 2010	Sheet 7 of 36	

PROJECT : ZQ2

Quanta Computer Inc.

For Check list JTAG

	R279	*4.7K_4	NB_PWRGD_IN
+3V	R88	*4.7K_4	INT_EDIDDATA
	R96	*4.7K_4	INT_EDIDCLK
+3V	R94	*4.7K_4	HDMI_DDC_DATA

All RS880 variants do not support analog TV-out functionality. As such, Y, C_Pr, and COMP_Pb

U16C — RS880/RX881 — PART 3 OF 6

Pin	Signal	Block
F12	AVDD2(NC)	CRT/TVOUT
E12	AVDD1(NC)	
F14	AVDDD(NC)	
G15	AVSSD(NC)	
H15	AVDDQ(NC)	
H14	AVSSQ(NC)	
E17	C_Pr(DFT_GPIO5)	
F17	Y(DFT_GPIO2)	
F15	COMP_Pb(DFT_GPIO4)	
G18	RED(DFT_GPIO0)	
G17	REDb(NC)	
E18	GREEN(DFT_GPIO1)	
F18	GREENb(NC)	
E19	BLUE(DFT_GPIO3)	
F19	BLUEb(NC)	
A11	DAC_HSYNC(PWM_GPIO4)	
B11	DAC_VSYNC(PWM_GPIO6)	
E8	DAC_SDA(PCE_TCALRN)	
F8	DAC_SCL(PCE_RCALRN)	
G14	DAC_RSET(PWM_GPIO1)	
A12	PLLVDD(NC)	PLL PWR
D14	PLLVDD18(NC)	
B12	PLLVSS(NC)	
H17	VDDA18HTPLL	
D7	VDDA18PCIEPLL1	
E7	VDDA18PCIEPLL2	
D8	SYSRESETb	PM
A10	POWERGOOD	
C10	LDTSTOPb	
C12	ALLOW_LDTSTOP	
C25	HT_REFCLKP	CLOCKs
C24	HT_REFCLKN	
E11	REFCLK_P/OSCIN(OSCIN)	
F11	REFCLK_N(PWM_GPIO3)	
T2	GFX_REFCLKP	
T1	GFX_REFCLKN	
U1	GPP_REFCLKP	
U2	GPP_REFCLKN	
V4	GPPSB_REFCLKP(SB_REFCLKP)	
V3	GPPSB_REFCLKN(SB_REFCLKN)	
A9	I2C_DATA	MIS.
B9	I2C_CLK	
B8	DDC_DATA/AUX0N(NC)	
A8	DDC_CLK/AUX0P(NC)	
B7	AUX1P(NC)	
A7	AUX1N(NC)	
B10	STRP_DATA	
G11	RSVD	
C8	AUX_CAL(NC)	
A22	TXOUT_L0P(NC)	
B22	TXOUT_L0N(NC)	
A21	TXOUT_L1P(NC)	
B21	TXOUT_L1N(NC)	
B20	TXOUT_L2P(NC)	
A20	TXOUT_L2N(DBG_GPIO0)	
A19	TXOUT_L3P(NC)	
B19	TXOUT_L3N(DBG_GPIO2)	
B18	TXOUT_U0P(NC)	
A18	TXOUT_U0N(NC)	
A17	TXOUT_U1P(PCIE_RESET_GPIO3)	
B17	TXOUT_U1N(PCIE_RESET_GPIO2)	
D20	TXOUT_U2P(NC)	
D21	TXOUT_U2N(NC)	
D18	TXOUT_U3P(PCIE_RESET_GPIO5)	
D19	TXOUT_U3N(NC)	
B16	TXCLK_LP(DBG_GPIO1)	
A16	TXCLK_LN(DBG_GPIO3)	
D16	TXCLK_UP(PCIE_RESET_GPIO4)	
D17	TXCLK_UN(PCIE_RESET_GPIO1)	
A13	VDDLTP18(NC)	LVTM
B13	VSSLTP18(NC)	
A15	VDDLT18_1(NC)	
B15	VDDLT18_2(NC)	
A14	VDDLT33_1(NC)	
B14	VDDLT33_2(NC)	
C14	VSSLT1(VSS)	
D15	VSSLT2(VSS)	
C16	VSSLT3(VSS)	
C18	VSSLT4(VSS)	
C20	VSSLT5(VSS)	
E20	VSSLT6(VSS)	
C22	VSSLT7(VSS)	
E9	LVDS_DIGON(PCE_TCALRP)	
E7	LVDS_BLON(PCE_RCALRP)	
G12	LVDS_ENA_BL(PWM_GPIO2)	
D9	TMDS_HPD(NC)	
D10	HPD(NC)	
D12	TVCLKIN(PWM_GPIO5)	
AE8	THERMALDIODE_P	
AD8	THERMALDIODE_N	
D13	TESTMODE	

VGA

[15] INT_CRT_RED	R102	140/F_4	
[15] INT_CRT_GRE	R103	150/F_4	
[15] INT_CRT_BLU	R104	150/F_4	
[15] INT_CRT_HSYNC	INT_CRT_HSYNC		
[15] INT_CRT_VSYNC	INT_CRT_VSYNC		
[15] INT_DDCDATA			
[15] INT_DDCCLK			
	R79	715/F_6	DAC_RSET_NB

+3V_AVDD_NB	F12	AVDD2(NC)
+1.8V_AVDDDI_NB	F14	AVDDD(NC)
+1.8V_AVDDQ_NB	H15	AVDDQ(NC)
+1.1V_PLLVDD	A12	PLLVDD(NC)
+1.8V_PLLVDD18	D14	PLLVDD18(NC)
	B12	PLLVSS(NC)
+1.8V_VDDA18HTPLL	H17	VDDA18HTPLL
+1.8V_VDDA18PCIEPLL	D7	VDDA18PCIEPLL1
	E7	VDDA18PCIEPLL2
[10,25] A_RST#_SB	D8	SYSRESETb
[2,11,14] NB_PWRGD_IN	A10	POWERGOOD
NB_LDT_STOP#	C10	LDTSTOPb
NB_ALLOW_LDTSTOP	C12	ALLOW_LDTSTOP
[10] CLK_NB_HTREFP_PR	C25	HT_REFCLKP
[10] CLK_NB_HTREFN_PR	C24	HT_REFCLKN
[10] CLK_NB_REF_CLKP	E11	REFCLK_P/OSCIN(OSCIN)
[10] CLK_NB_REF_CLKN	F11	REFCLK_N(PWM_GPIO3)
R46 4.7K_4	T2	GFX_REFCLKP
R45 4.7K_4	T1	GFX_REFCLKN
T15	U1	GPP_REFCLKP
T13	U2	GPP_REFCLKN
[10] CLK_SBLINKP	V4	GPPSB_REFCLKP(SB_REFCLKP)
[10] CLK_SBLINKN	V3	GPPSB_REFCLKN(SB_REFCLKN)
[15] INT_EDIDDATA	A9	I2C_DATA
[15] INT_EDIDCLK	B9	I2C_CLK
[16] HDMI_DDC_DATA	B8	DDC_DATA/AUX0N(NC)
[16] HDMI_DDC_CLK	A8	DDC_CLK/AUX0P(NC)
[30] +NB_CORE_ON	+NB_CORE_ON B10	STRP_DATA
T74	RS880_AUX_CAL C8	AUX_CAL(NC)

20mA — +1.8V_VDDA18HTPLL
120mA — +1.8V_VDDA18PCIEPLL

LA_DATAP0 [15]	A22	TXOUT_L0P(NC)
LA_DATAN0 [15]	B22	TXOUT_L0N(NC)
LA_DATAP1 [15]	A21	TXOUT_L1P(NC)
LA_DATAN1 [15]	B21	TXOUT_L1N(NC)
LA_DATAP2 [15]	B20	TXOUT_L2P(NC)
LA_DATAN2 [15]	A20	TXOUT_L2N(DBG_GPIO0)
	A19	TXOUT_L3P(NC)
	B19	TXOUT_L3N(DBG_GPIO2)
	B18	TXOUT_U0P(NC)
	A18	TXOUT_U0N(NC)
	A17	TXOUT_U1P(PCIE_RESET_GPIO3)
	B17	TXOUT_U1N(PCIE_RESET_GPIO2)
	D20	TXOUT_U2P(NC)
	D21	TXOUT_U2N(NC)
	D18	TXOUT_U3P(PCIE_RESET_GPIO5)
	D19	TXOUT_U3N(NC)
LA_CLK [15]	B16	TXCLK_LP(DBG_GPIO1)
LA_CLK# [15]	A16	TXCLK_LN(DBG_GPIO3)
	D16	TXCLK_UP(PCIE_RESET_GPIO4)
	D17	TXCLK_UN(PCIE_RESET_GPIO1)
	A13	VDDLTP18(NC)
	B13	VSSLTP18(NC)
	A15	VDDLT18_1(NC)
	B15	VDDLT18_2(NC)
	A14	VDDLT33_1(NC)
	B14	VDDLT33_2(NC)
	C14	VSSLT1(VSS)
	D15	VSSLT2(VSS)
	C16	VSSLT3(VSS)
	C18	VSSLT4(VSS)
	C20	VSSLT5(VSS)
	E20	VSSLT6(VSS)
	C22	VSSLT7(VSS)
INT_LVDS_DIGON [15]	E9	LVDS_DIGON(PCE_TCALRP)
INT_DPST_PWM [15]	E7	LVDS_BLON(PCE_RCALRP)
INT_LVDS_BLON [15]	G12	LVDS_ENA_BL(PWM_GPIO2)
INT_HDMI_HPD [16]	D9	TMDS_HPD(NC)
	D10	HPD(NC)
SUS_STAT# [11]	D12	TVCLKIN(PWM_GPIO5)
	AE8	THERMALDIODE_P
	AD8	THERMALDIODE_N
	D13	TESTMODE

+1.8V_VDDLTP18_NB — 15mA
+1.8V_VDDLT_18_NB — 300mA

R111 *0short_4 — SUS_STAT# NB
R112 *3K_4
R87 1.8K/F_4

Made provision for external pull-down which is not installed by default. Pulled up externally for bypassing EEPROM strapping and using default values.

DDC_DATA & DDC_CLK Not applicable to RX881

For A11 version

(02/10) Don~t need 49.9 ohm PD.

R47	*49.9/F_4	CLK_SBLINKP
R48	*49.9/F_4	CLK_SBLINKN

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

RS880M	
1 Disable	V
0 Enable	

INT_CRT_VSYNC — R277 3K_4 — +3V

RS880M: Enables Side port memory

RS880M:INT_CRT_HSYNC

Selects if Memory SIDE PORT is available or not

1 = Memory Side port Not available

0 = Memory Side port available

Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

INT_CRT_HSYNC — R276 *SP@3K_4 — +3V
R100 SIDE@3K_4

For extrnal EEPROM Debug only

RS780/RX780/RS880

+NB_CORE_ON — R278 2K/F_4

Display Port interface from PCIeGraphics (RS880/rs880M only)

RS880_AUX_CAL — R282 *150/F_4

RS880M --- ADD

+3V — L11 BLM18PG221SN1D(220_1.4A)_6 — +3V_AVDD_NB
C120 *10u/6.3V_8
C123 2.2U/6.3V_6
AVDD-DAC Analog not applicable to RX780

+1.1V — L39 BLM18PG221SN1D(220_1.4A)_6 — +1.1V_PLLVDD
C359 2.2U/6.3V_6
PLLVDD - Graphics PLL not applicable to RX780

+1.8V — L15 BLM18PG221SN1D(220_1.4A)_6 — +1.8V_VDDLTP18_NB
C135 2.2U/6.3V_6
VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780

L40 BLM21PG221SN1D(220,100M,2A)_8 — +1.8V_VDDLT_18_NB
C360 4.7u/6.3V_6
C357 .1u/10V_4
VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780

+1.8V — R86 0_6 — +1.8V_AVDDDI_NB
C113 .1u/10V_4
AVDDI-DAC Digital not applicable to RX780

+1.8V — L13 BLM18PG221SN1D(220_1.4A)_6 — +1.8V_PLLVDD18
C147 *10u/6.3V_8
C128 4.7u/6.3V_6
PLLVDD18 - Graphics PLL not applicable to RX780

L9 BLM18PG221SN1D(220_1.4A)_6 — +1.8V_AVDDQ_NB
C108 2.2U/6.3V_6
AVDDQ-DAC Bandgap Reference not applicable to RX780

+1.8V — L10 BLM18PG221SN1D_6 — +1.8V_VDDA18PCIEPLL
VDDA18PCIEPLL -PCIE PLL — 20mils width
C122 2.2U/6.3V_6

VDDA18HTPLL -HT LINK PLL — 20mils width
L14 BLM18PG221SN1D_6 — +1.8V_VDDA18HTPLL
C106 2.2U/6.3V_6

+1.8V — U6 — 74LVC07 (Open Drain)
[2,10] CPU_LDT_STOP# — NB_LDT_STOP#
+1.8V — R107 2.2K_4 — 9/16 need modify PN

DDR3 based CPU : Level shifted to 1.8 V on the Northbridge side using an open-drain buffer and pulled up to 1.8V_S0 through a 2.2k Ohm 5% resistor on the Northbridge side.

R285 1K_4 — +1.8V
[2] CPU_LDT_REQ# — R284 *0_4 — NB_ALLOW_LDTSTOP
[10] ALLOW_LDTSTOP — R283 0_4

The RS880 family does not support CLMC architecture
The LDTREQ# connection from the CPU to ALLOW_LDTSTOP of the Northbridge is no longer required.

PROJECT : ZQ2		
Quanta Computer Inc.		
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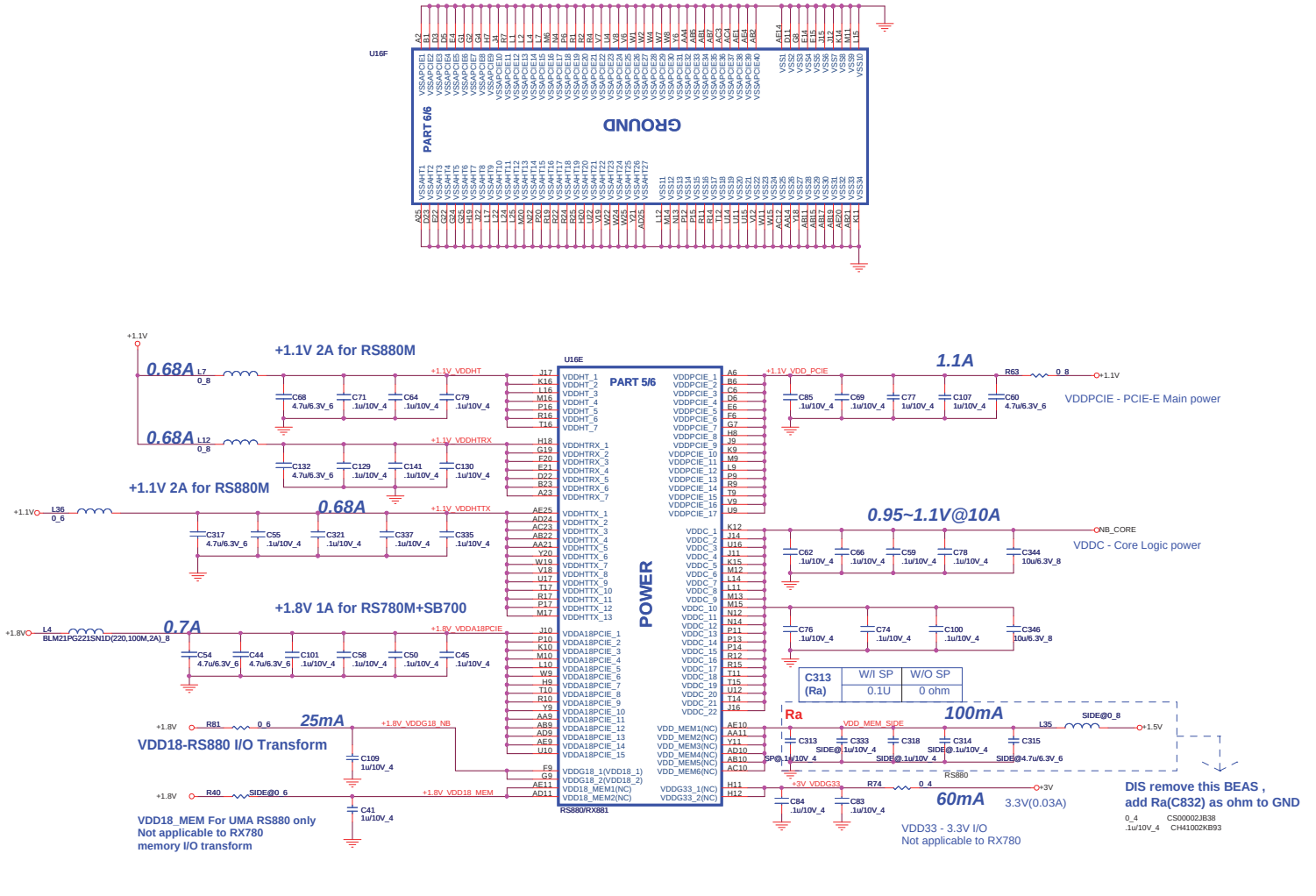
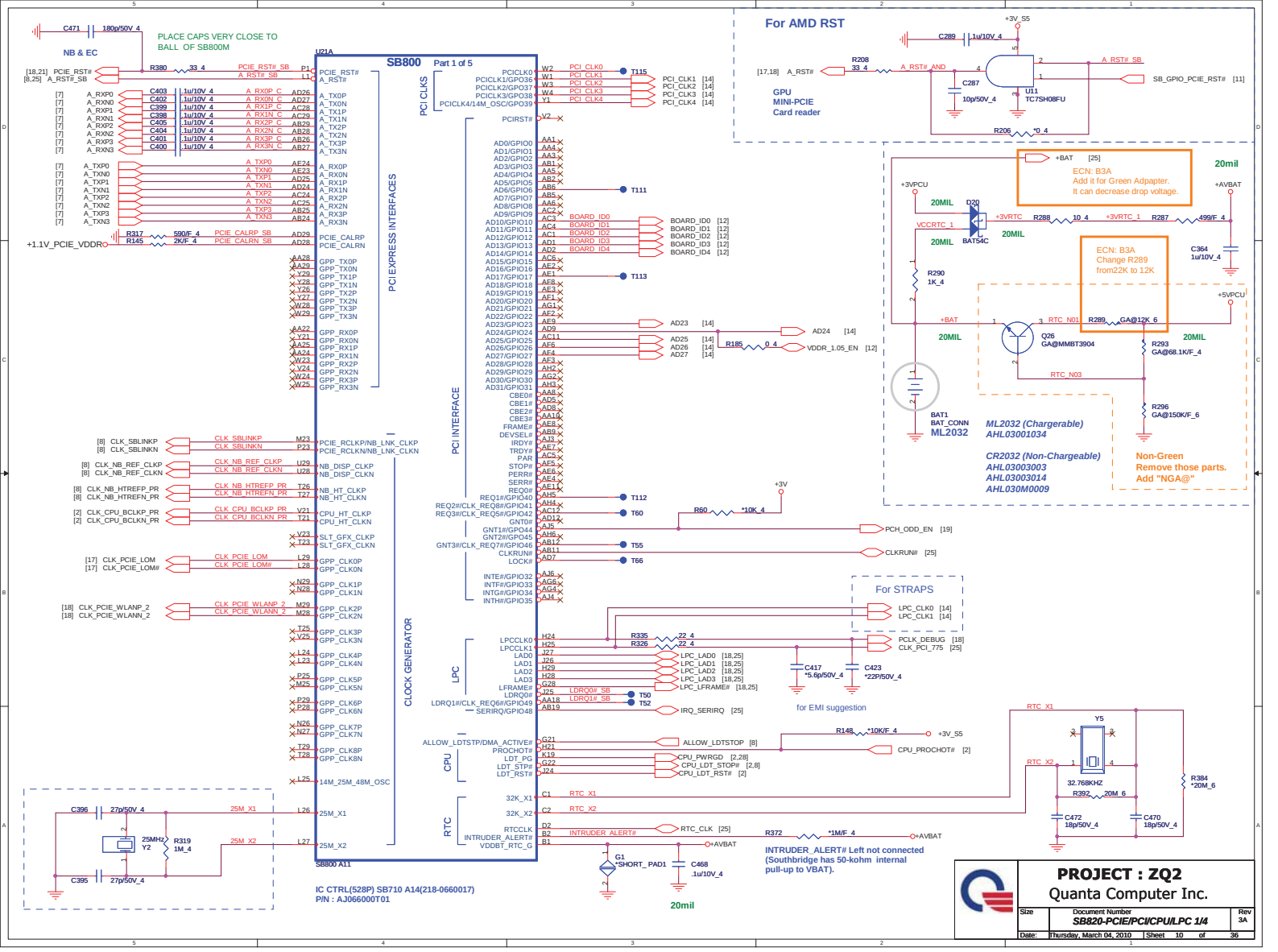


C313 (Ra)	W/I SP	W/O SP
	0.1U	0 ohm


SB800
Part 1 of 5
U21A
PCI CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
NB & EC
PLACE CAPS VERY CLOSE TO BALL OF SB800M
For AMD RST
GPU
MINI-PCIE
Card reader
U11
TC7SH08FU
ECN: B3A
Add it for Green Adpapter.
It can decrease drop voltage.
ECN: B3A
Change R289
from22K to 12K
Q26
GA@MMBT3904
BAT1
BAT_CONN
ML2032
ML2032 (Chargerable)
AHL03001034
CR2032 (Non-Chargeable)
AHL03003003
AHL03003014
AHL030M0009
Non-Green
Remove those parts.
Add "NGA@"
For STRAPS
for EMI suggestion
Y5
32.768KHZ
Y2
25MHz
INTRUDER_ALERT# Left not connected
(Southbridge has 50-kohm internal
pull-up to VBAT).
IC CTRL(528P) SB710 A14(218-0660017)
P/N : AJ066000T01
SB800 A11
PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number
SB820-PCIE/PCI/CPU/LPC 1/4
Rev
3A
Date: Thursday, March 04, 2010
Sheet 10 of 36

NC only ,Can't be install

+3V_S5
R368 *2.2K_4 SB_TEST0
R217 *2.2K_4 SB_TEST1
R210 *2.2K_4 SB_TEST2

SCL0/SDATA0 is 3V tolerance. AMD datasheet define it
Clk Gen/ Robson/ TV tuner/ DDR2/ Thermal/ Accelerometer

+3V
R150 2.2K_4 PCLK_SMB
R147 2.2K_4 PDAT_SMB

SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it

+3V_S5
R188 10K_4 SB_SMBCLK1
R215 10K_4 SB_SMBDATA1

SCL2/SDATA2 is 3V/S5 tolerance.
AMD datasheet define it

+3V_S5
R153 10K_4 SB_SCLK2
R149 10K_4 SB_SDATA2

+3V
R195 4.7K_4 SUS_STAT#

+3V
R316 8.2K_4 CLK_PCIE_LAN_REQ#
R178 8.2K_4 CLK_PCIE_2_REQ#

JTAG DEBUG

CN13 (+3V_S5, C279 10P/50V_4)
1 SB_JTAG_TCK
2 SB_JTAG_TDO
3 SB_JTAG_TDI
4 SB_TEST1
5
6 SB_JTAG_RST#
7
8

*S/W JTAG DEBUG

To Azalia

ACZ_SDOUT R200 33_4 ACZ_SDOUT_AUDIO [20]
C283 *10P/50V_4
ACZ_SYNC R202 33_4 ACZ_SYNC_AUDIO [20]
C284 *10P/50V_4
ACZ_BCLK R203 33_4 ACZ_BITCLK_AUDIO [20]
C285 *10P/50V_4
ACZ_RST# R201 33_4 ACZ_RST#_AUDIO [20]
ACZ_SDIN0 ACZ_SDIN0 [20]

USBCLK/41M_25M_48M_OSC pin is CLK input pin when EXT CLKGEN mode.
It is output CLK source when INT CLKGEN mode.

U21D

SB800
Part 4 of 5

ACPI / WAKE UP EVENTS

Pin	Signal	Net
J2	PCI_PME#/GEVENT4#	SB_PCI_PME#
K1	RI#/GEVENT22#	
D3	SPI_CS3#/GBE_STAT1/GEVENT21#	
F1	SLP_S3#	SUSB# [25]
H1	SLP_S5#	SUSC# [25]
E2	PWR_BTN#	DNBSWON# [25]
H5	PWR_GOOD	SB_PWRGD_IN [14]
G6	SUS_STAT#	SUS_STAT# [8]
B3	TEST0	SB_TEST0
C4	TEST1/TMS	SB_TEST1
F6	TEST2	SB_TEST2
AD21	GA20IN/GEVENT0#	SIO_A20GATE [25]
AE21	KBRST#/GEVENT1#	SIO_RCIN# [25]
K2	LPC_PME#/GEVENT3#	LANLINK_STATE# T114
J29	LPC_SMI#/GEVENT23#	SIO_EXT_SMI# [25]
H2	GEVENTS#	SIO_EXT_SCI# [25]
J1	SYS_RESET#/GEVENT19#	SYS_RST# T116
H6	WAKE#/GEVENT8#	PCIE_WAKE# [17,18]
F3	IR_RX1/GEVENT20#	IR_RX1 T117
J6	THRMTRIP#/SMBALERT#/GEVENT2#	SB_THERMTRIP# T69
AC19	NB_PWRGD	NB_PWRGD_IN [2,8,14]
G1	RSMRST#	ICH_RSMRST# [25]

USB 1.1 USB MISC

Pin	Signal	Net
J10	USB_FSD1P/GPIO186	
H11	USB_FSD1N	
H9	USB_FSD2P/GPIO185	USB_FDS12P T63
J8	USB_FSD2N	USB_FDS12N T58

GPIO

Pin	Signal	Net
AD19	CLK_REQ4#/SATA_IS0#/GPIO64	
AA16	CLK_REQ3#/SATA_IS1#/GPIO63	
AB21	SMARTVOLT1/SATA_IS2#/GPIO50	SB_GPIO_PCIE_RST# [10]
AC18	CLK_REQ0#/SATA_IS3#/GPIO60	CLK_PCIE_LAN_REQ# [17]
AF20	SATA_IS4#/FANOUT3/GPIO55	
AE19	SATA_IS5#/FANIN3/GPIO59	SB_GPIO59 T51
AF19	SPKR/GPIO66	SPKR [20]
AD22	SCL0/GPIO43	PCLK_SMB [5,17,18]
AE22	SDA0/GPIO47	PDAT_SMB [5,17,18]
F5	SCL1/GPIO227	SB_SMBCLK1
F4	SDA1/GPIO228	SB_SMBDATA1
AH21	CLK_REQ2#/FANIN4/GPIO62	CLK_PCIE_2_REQ# [18]
AB18	CLK_REQ1#/FANOUT4/GPIO61	
E1	IR_LED#/LLB#/GPIO184	
AJ21	SMARTVOLT2/SHUTDOWN#/GPIO51	
H4	DDR3_RST#/GEVENT7#	SP_DDR3_RST# [6]
D5	GBE_LED0/GPIO183	
D7	GBE_LED1/GEVENT9#	
G5	GBE_LED2/GEVENT10#	
K3	GBE_STAT0/GEVENT11#	
AA20	CLK_REQG#/GPIO65/OSCIN	E_SB_OSC T109

USB OC

Pin	Signal	Net
H3	BLINK/USB_OC7#/GEVENT18#	OC_7# [22]
D1	USB_OC6#/IR_TX1/GEVENT6#	OC_6# [22]
E4	USB_OC5#/IR_TX0/GEVENT17#	SB_PM_THERM# T59
D4	USB_OC4#/IR_RX0/GEVENT16#	OC_4# [22]
E8	USB_OC3#/AC_PRES/TDO/GEVENT15#	SB_JTAG_TDO
F7	USB_OC2#/TCK/GEVENT14#	SB_JTAG_TCK
E7	USB_OC1#/TDI/GEVENT13#	SB_JTAG_TDI
F8	USB_OC0#/TRST#/GEVENT12#	SB_JTAG_RST#

Eliot (02/26)
Current Agesa bios doesn't program ALERT_L and SB won't process alert.

HD audio interface is +3VS5 voltage

HD AUDIO

Pin	Signal	Net
M3	AZ_BITCLK	ACZ_BCLK
N1	AZ_SDOUT	ACZ_SDOUT
L2	AZ_SDIN0/GPIO167	ACZ_SDIN0
M2	AZ_SDIN1/GPIO168	
M1	AZ_SDIN2/GPIO169	
M4	AZ_SDIN3/GPIO170	
N2	AZ_SYNC	ACZ_SYNC
P2	AZ_RST#	ACZ_RST#

GBE LAN

Pin	Signal	Net
T1	GBE_COL	GBE_COL
T4	GBE_CRS	GBE_CRS
L6	GBE_MDCK	
L5	GBE_MDIO	GBE_MDIO
T9	GBE_RXCLK	
U1	GBE_RXD3	
U3	GBE_RXD2	
T2	GBE_RXD1	
U2	GBE_RXD0	
T5	GBE_RXCTL/RXDV	
V5	GBE_RXERR	GBE_RXERR
P5	GBE_TXCLK	
M5	GBE_TXD3	
P9	GBE_TXD2	
T7	GBE_TXD1	
P7	GBE_TXD0	
M7	GBE_TXCTL/TXEN	
P4	GBE_PHY_PD	
M9	GBE_PHY_RST#	
V7	GBE_PHY_INTR	GBE_PHY_INTR

EMBEDDED CTRL

Pin	Signal	Net
E23	PS2_DAT/SDA4/GPIO187	ADP_PRES0 T49
E24	PS2_CLK/SCL4/GPIO188	
F21	SPI_CS2#/GBE_STAT2/GPIO166	
G29	FC_RST#/GPIO160	
D27	PS2KB_DAT/GPIO189	
F28	PS2KB_CLK/GPIO190	
F29	PS2M_DAT/GPIO191	
E27	PS2M_CLK/GPIO192	

[02/22] AMD FAE and checklist request PL.

SB800 A11

USB 2.0

Pin	Signal	Net	Port	Bits
A10	USB_14_48M	T110		
G19	USB_RCOMP_SB	R169 11.8K/F_6		
B12	USB_HSD13P	USBP13+ [15]	CAMERA	
A12	USB_HSD13N	USBP13- [15]	CAMERA	
F11	USB_HSD12P	USBP12+ [22]	USBX3 board	
E11	USB_HSD12N	USBP12- [22]	USBX3 board	
E14	USB_HSD11P	USBP11+ [22]	USBX3 board	
E12	USB_HSD11N	USBP11- [22]	USBX3 board	
J12	USB_HSD10P	USBP10+ [21]	Card reader	
J14	USB_HSD10N	USBP10- [21]	Card reader	
A13	USB_HSD9P	USBP9+ [22]	BLUETOOTH	
B13	USB_HSD9N	USBP9- [22]	BLUETOOTH	
D13	USB_HSD8P	USBP8+ [22]	USBX3 board	
C13	USB_HSD8N	USBP8- [22]	USBX3 board	
G12	USB_HSD7P			
G14	USB_HSD7N			
G16	USB_HSD6P			
G18	USB_HSD6N			
D16	USB_HSD5P			
C16	USB_HSD5N			
B14	USB_HSD4P	USBP4+ [18]	WLAN Min-Card	
A14	USB_HSD4N	USBP4- [18]	WLAN Min-Card	
E18	USB_HSD3P			
E16	USB_HSD3N			
J16	USB_HSD2P			
J18	USB_HSD2N			
B17	USB_HSD1P	USBP1+ T54		
A17	USB_HSD1N	USBP1- T53		
A16	USB_HSD0P	USBP0+ [22]		
B16	USB_HSD0N	USBP0- [22]		

EHCI3/ OHCI3
EHCI2/ OHCI2
EHCI1/ OHCI1

On Board USB Connector
Only USB Port0 can be configured as debug port.

EMBEDDED CTRL

Pin	Signal	Net
D25	SCL2/GPIO193	SB_SCLK2
F23	SDA2/GPIO194	SB_SDATA2
B26	SCL3_LV/GPIO195	SB_GPIO195
E26	SDA3_LV/GPIO196	SB_GPIO196
F25	EC_PWM0/EC_TIMER0/GPIO197	T48
E22	EC_PWM1/EC_TIMER1/GPIO198	
F22	EC_PWM2/EC_TIMER2/GPIO199	GPIO199 [14]
E21	EC_PWM3/EC_TIMER3/GPIO200	GPIO200 [14]
G24	KSI_0/GPIO201	
G25	KSI_1/GPIO202	
E28	KSI_2/GPIO203	
E29	KSI_3/GPIO204	
D29	KSI_4/GPIO205	
D28	KSI_5/GPIO206	
C29	KSI_6/GPIO207	
C28	KSI_7/GPIO208	
B28	KSO_0/GPIO209	
A27	KSO_1/GPIO210	
B27	KSO_2/GPIO211	
D26	KSO_3/GPIO212	
A26	KSO_4/GPIO213	
C26	KSO_5/GPIO214	
A24	KSO_6/GPIO215	
B25	KSO_7/GPIO216	
A25	KSO_8/GPIO217	
D24	KSO_9/GPIO218	
B24	KSO_10/GPIO219	
C24	KSO_11/GPIO220	
B23	KSO_12/GPIO221	
A23	KSO_13/GPIO222	
D22	KSO_14/GPIO223	
C22	KSO_15/GPIO224	
A22	KSO_16/GPIO225	
B22	KSO_17/GPIO226	

Check list

SB_GPIO195 R146 10K_4
SB_GPIO196 R144 10K_4

PROJECT : ZQ2
Quanta Computer Inc.

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	SB820-ACPI/GPIO/USB 2/4	1A

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Max trace length: 6"

SATA HDD

[19] SATA_TX0+ — C248 .01u/16V_4 — SATA_TX0+_C — AH9 SATA_TX0P
[19] SATA_TX0- — C245 .01u/16V_4 — SATA_TX0-_C — AJ9 SATA_TX0N
[19] SATA_RX0- — AJ8 SATA_RX0N
[19] SATA_RX0+ — AH8 SATA_RX0P

SATA ODD

[19] SATA_TX1+ — C103 .01u/16V_4 — SATA_TX1+_C — AH10 SATA_TX1P
[19] SATA_TX1- — C82 .01u/16V_4 — SATA_TX1-_C — AJ10 SATA_TX1N
[19] SATA_RX1- — AG10 SATA_RX1N
[19] SATA_RX1+ — AF10 SATA_RX1P

AG12 SATA_TX2P
AF12 SATA_TX2N
AJ12 SATA_RX2N
AH12 SATA_RX2P
AH14 SATA_TX3P
AJ14 SATA_TX3N
AG14 SATA_RX3N
AF14 SATA_RX3P
AG17 SATA_TX4P
AF17 SATA_TX4N
AJ17 SATA_RX4N
AH17 SATA_RX4P
AJ18 SATA_TX5P
AH18 SATA_TX5N
AH19 SATA_RX5N
AJ19 SATA_RX5P

SATA PORT 0,1,2,3 can support AHCI mode

Signal Name	Explanation
SATA_CALRP	SB800 A11: 800 ohm 1% resistor to GND. SB800 A12: 1K ohm 1% resistor to GND.
SATA_CALRN	SB800 A11: 931 ohm 1% resistor to VDDAN_11_SATA. SB800 A12: 931 ohm 1% resistor to VDDAN_11_SATA.

E-SATA

+1.1V_AVDD_SATA — R170 1K/F_4 — SATA_CALRP — AB14 SATA_CALRP
R166 931/F_4 — SATA_CALRN — AA14 SATA_CALRN

[22] SATA_ACT# — AD11 SATA_ACT#/GPIO67
+3V — R175 10K_4

C436 *27p/50V_4 — SATA_X1 — AD16 SATA_X1
Y3 *25MHz — R338 *1M_4
C424 *27p/50V_4 — SATA_X2 — AC16 SATA_X2

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB820

T61 — SB_GPIO164 — J5 SPI_DI/GPIO164
T64 — SB_GPIO163 — E2 SPI_DO/GPIO163
T72 — SB_GPIO162 — K4 SPI_CLK/GPIO162
T56 — SB_GPIO165 — K9 SPI_CS1#/GPIO165
T73 — SB_GPIO161 — G2 ROM_RST#/GPIO161

U21B — SB800 — Part 2 of 5 — SB800 A11

SERIAL ATA

FLASH:
FC_CLK — AH28 — T82
FC_FBCLKOUT — AG28 — T79
FC_FBCLKIN — AE26 — T76
FC_OE#/GPIO0145 — AF28 — T81
FC_AVD#/GPIO0146 — AG29 — T75
FC_WE#/GPIO0148 — AG26 — T83
FC_CE1#/GPIO0149 — AF27 — T77
FC_CE2#/GPIO0150 — AE29 — T80
FC_INT1/GPIO0144 — AF29 — T78
FC_INT2/GPIO0147 — AH27 — T84
FC_ADQ0/GPIO0128 — AJ27 — T85
FC_ADQ1/GPIO0129 — AJ26 — T87
FC_ADQ2/GPIO0130 — AH25 — T91
FC_ADQ3/GPIO0131 — AH24 — T89
FC_ADQ4/GPIO0132 — AG23 — T94
FC_ADQ5/GPIO0133 — AH23 — T96
FC_ADQ6/GPIO0134 — AJ22 — T98
FC_ADQ7/GPIO0135 — AG21 — T106
FC_ADQ8/GPIO0136 — AF21 — T101
FC_ADQ9/GPIO0137 — AH22 — T99
FC_ADQ10/GPIO0138 — AJ23 — T95
FC_ADQ11/GPIO0139 — AF23 — T93
FC_ADQ12/GPIO0140 — AJ24 — T92
FC_ADQ13/GPIO0141 — AJ25 — T90
FC_ADQ14/GPIO0142 — AG25 — T88
FC_ADQ15/GPIO0143 — AH26 — T86

IF THERE IS NO IDE_TEST POINTS FOR DEBUG BUS IS MANDATORY

HW MONITOR:
FANOUT0/GPIO052 — W5
FANOUT1/GPIO053 — W6
FANOUT2/GPIO054 — Y9 — BT_OFF# — T68
FANIN0/GPIO056 — W7 — WWAN_DET# — T70
FANIN1/GPIO057 — V9 — CPPE_NC1# — T62
FANIN2/GPIO58 — W8 — CRD_REQ1# — T67
TEMPIN0/GPIO171 — B6 — TEMPIN0
TEMPIN1/GPIO172 — A6 — TEMPIN1
TEMPIN2/GPIO173 — A5 — MB_THRMDA_SB
TEMPIN3/TALERT#/GPIO174 — B5 — SB_GPIO174
TEMP_COMM — C7 — TEMP_COMM — R176 *0/short_4
VIN0/GPIO175 — A3 — SB_GPIO175
VIN1/GPIO176 — B4 — SB_GPIO176
VIN2/GPIO177 — A4 — SIDE_PORT_ID0
VIN3/GPIO178 — C5 — SIDE_PORT_ID1
VIN4/GPIO179 — A7 — MEM_1V5
VIN5/GPIO180 — B7 — SB820_GPIO180 — T65
VIN6/GBE_STAT3/GPIO181 — B8 — SB820_GPIO182
VIN7/GBE_LED3/GPIO182 — A8 — T57

SPI ROM:
NC1 — G27
NC2 — Y2

Check list

TEMPIN0 — R346 — 10K_4
TEMPIN1 — R345 — 10K_4
MB_THRMDA_SB — R350 — 10K_4
SB_GPIO174 — R353 — 10K_4
SB_GPIO175 — R364 — 10K_4
SB_GPIO176 — R366 — 10K_4

BOM check

+3V — R374 *10K_4 — BOARD_ID0 — R385 10K_4
R375 *10K_4 — BOARD_ID1 — R386 10K_4
R377 SP@10K_4 — BOARD_ID2 — R388 *SP@10K_4
R376 SP@10K_4 — BOARD_ID3 — R387 *SP@10K_4
R378 10K_4 — BOARD_ID4 — R389 *10K_4

[10] BOARD_ID0 — BOARD_ID0
[10] BOARD_ID1 — BOARD_ID1
[10] BOARD_ID2 — BOARD_ID2
[10] BOARD_ID3 — BOARD_ID3
[10] BOARD_ID4 — BOARD_ID4

	1	0
ID0	15"	14"
ID1	DIS	UMA
ID2	W/I	W/O
ID3	JM	JV
ID4	6L	8L

Sideport

+3V_S5 — R177 *SP@10K_4 — SIDE_PORT_ID0 — R356 SP@10K_4
R193 *10K_4 — SIDE_PORT_ID1 — R359 10K_4

	1	0
ID0	SAM	HYU
ID1	RSV	RSV

DDR3 Sideport Memory Device

Vendor	*Vendor P/N*	*STN B/S P/N*	*Size*	*BOARD_ID2 GPIO12*	*SIDE_PORT_ID1 GPIO178*	*SIDE_PORT_ID0 GPIO177*
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB	0 (WO/Sideport)	0	0
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB	1 (W/Sideport)	0	1

+3V — PC68 .1u/10V_4
U10 TC7SH08FU
MEM_1V5 — 2
[10] VDDR_1.05_EN — 1
4 — VDDR_OPT [31]
PR91 *0_4

VDDR_1.05_EN:
1 : VDDR =1.05V
0 : VDDR = 0.9V (Default)

PROJECT : ZQ2
Quanta Computer Inc.

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	SB820-SATA/IDE/SPI 3/4	1A

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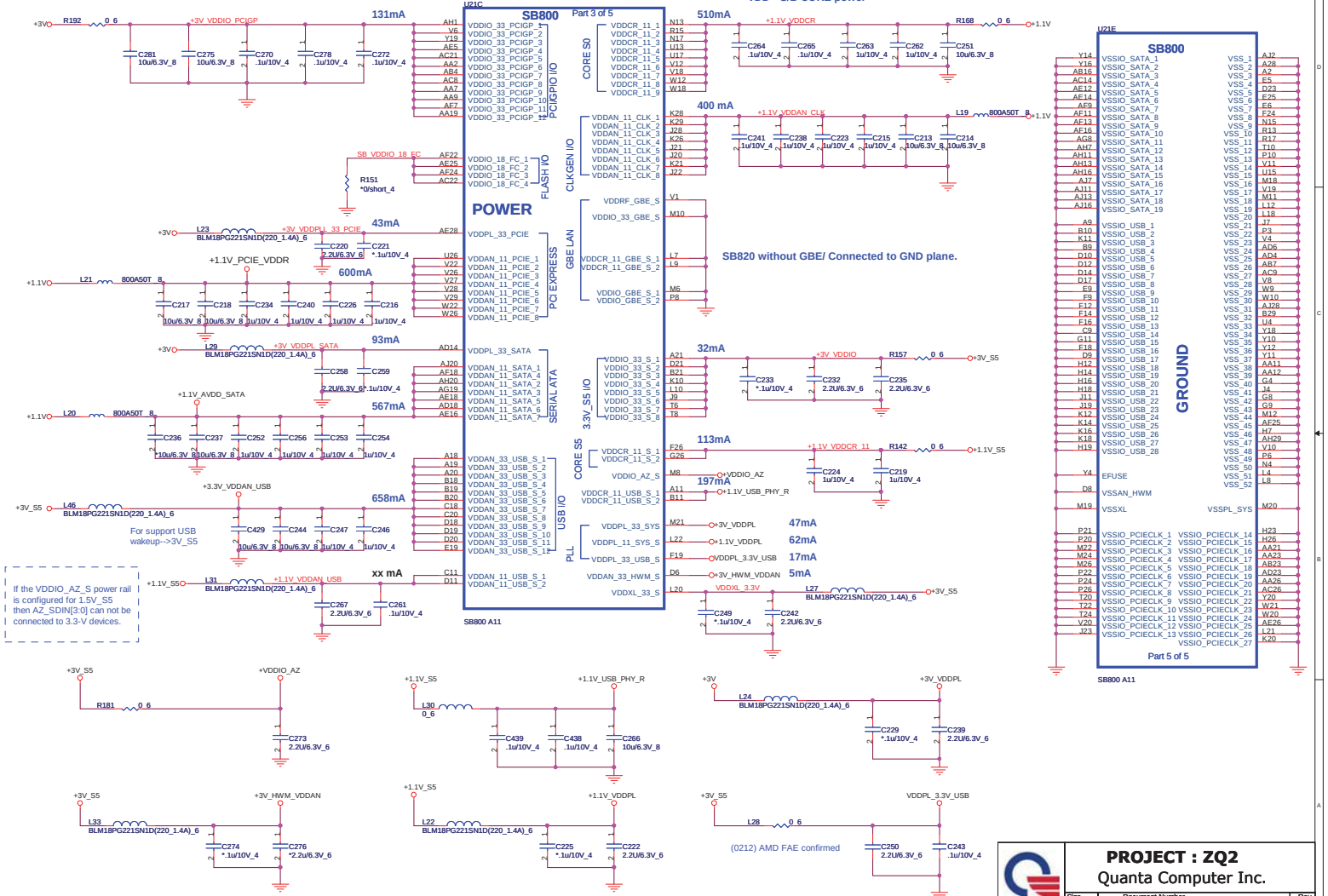
VDDQ--3.3V I/O power
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
VDD-- S/B CORE power
U21C
SB800
Part 3 of 5
POWER
PCI/GPIO I/O
FLASH I/O
PCI EXPRESS
SERIAL ATA
USB I/O
CORE S0
CLKGEN I/O
GBE LAN
3.3V_S5 I/O
CORE S5
PLL
131mA
43mA
600mA
93mA
567mA
658mA
xx mA
510mA
400 mA
32mA
113mA
197mA
47mA
62mA
17mA
5mA
+1.1V_PCIE_VDDR
SB820 without GBE/ Connected to GND plane.
For support USB wakeup-->3V_S5
If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.
SB800 A11
U21E
SB800
GROUND
Part 5 of 5
SB800 A11
(0212) AMD FAE confirmed
PROJECT : ZQ2
Quanta Computer Inc.
Size
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SB820-PWR/DECOUPLING 4/4
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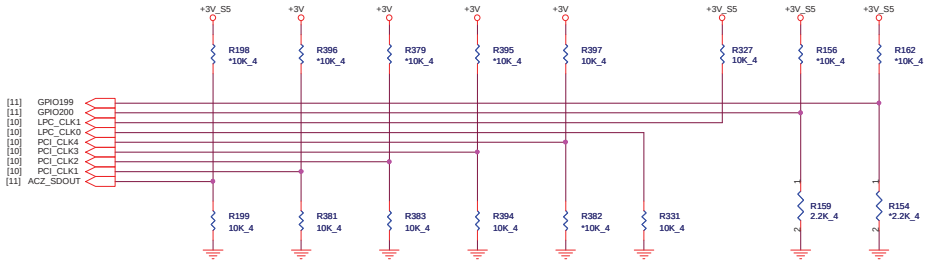
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

SB820M is supported Gen.1 mode only.

For internal clock GEN.

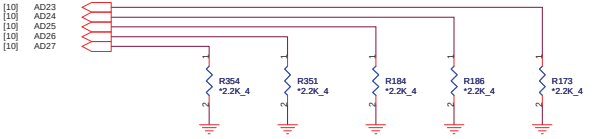


	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H=LPC ROM DEFAULT L, L=FWH ROM

internal have
pull Hi 10K

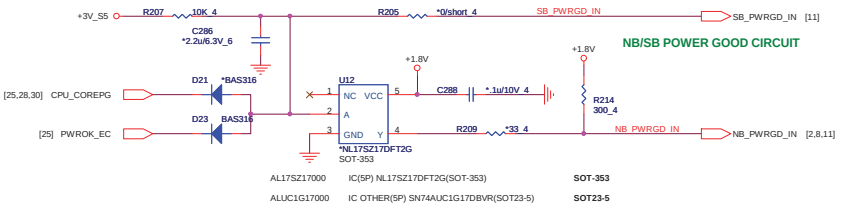
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353

ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

PROJECT : ZQ2

Quanta Computer Inc.

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	SB820-STRAPS	1A

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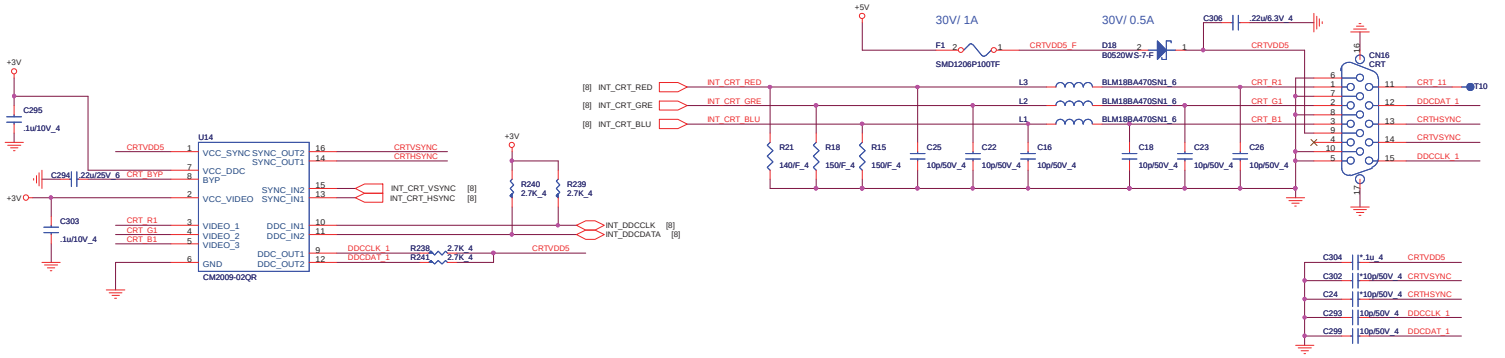
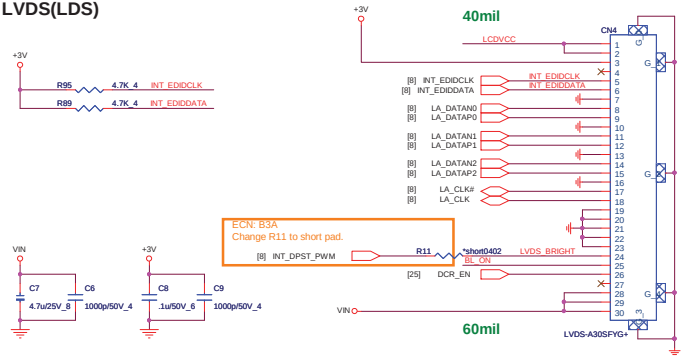
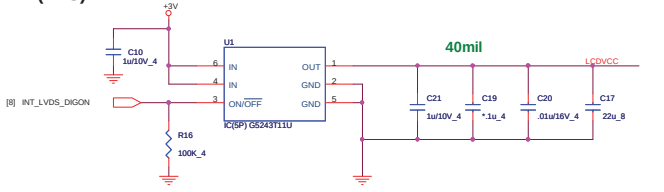
CRT



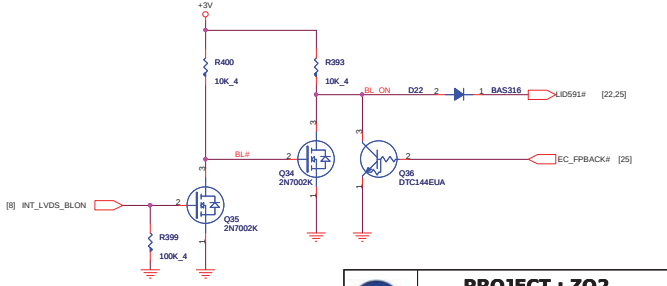
LVDS(LDS)



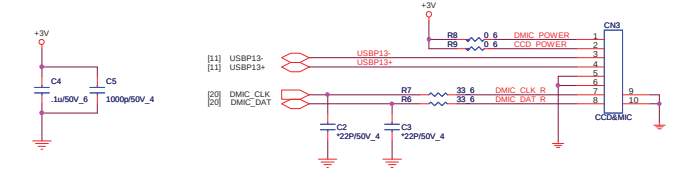
LCD PW(LDS)



Backlight Control(LDS)



CAMERA Module(CCD)



PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	CRT/LVDS/LID	3A

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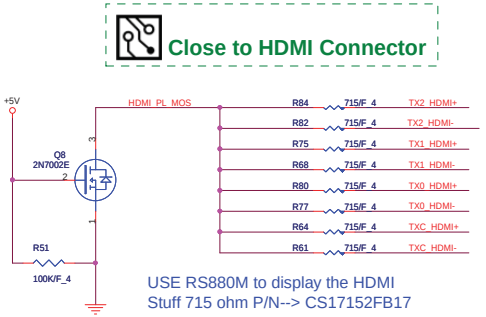
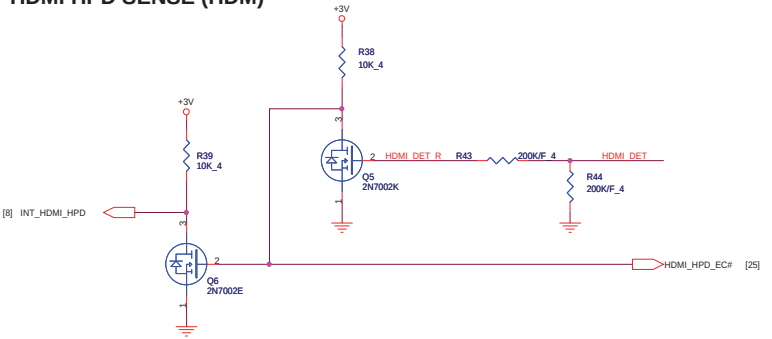
HDMI (HDM)

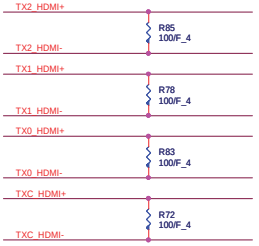


HDMI HPD SENSE (HDM)



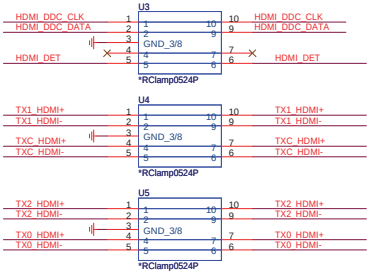
EMI reserve for HDMI(EMC)

Close connector

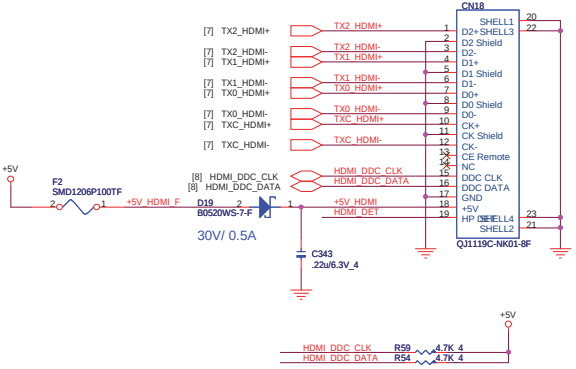


ESD Protect (EMC)

close to HDMI connector



HDMI PORT (HDM)



PROJECT : ZQ2

Quanta Computer Inc.

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	HDMI	1A

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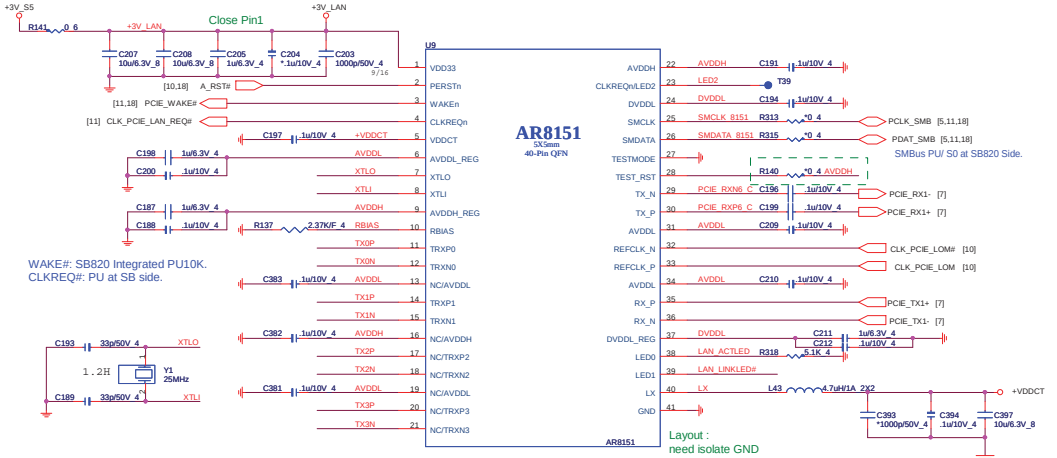
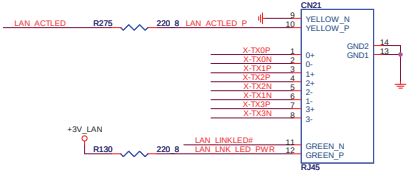
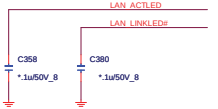
Giga-LAN AR8151



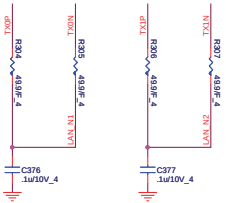
RJ45(LAN)



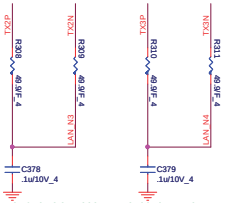


Sertek (03/01):
EMI capacitors, 470pF is enough.
Don't over 490 pF.

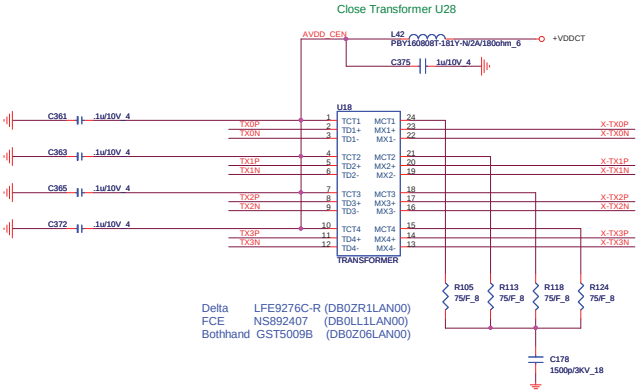
TRANSFORMER(LAN)



(03/02) Nick: Width trace behind capacitors.



(03/02) Nick: Width trace behind capacitors.



Delta LFE9276C-R (DB0ZR1LAN00)
FCE NS892407 (DB0LL1LAN00)
Bothhand GST5009B (DB0Z06LAN00)

PROJECT : ZQ2
Quanta Computer Inc.

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	LAN (AR8151)	1A

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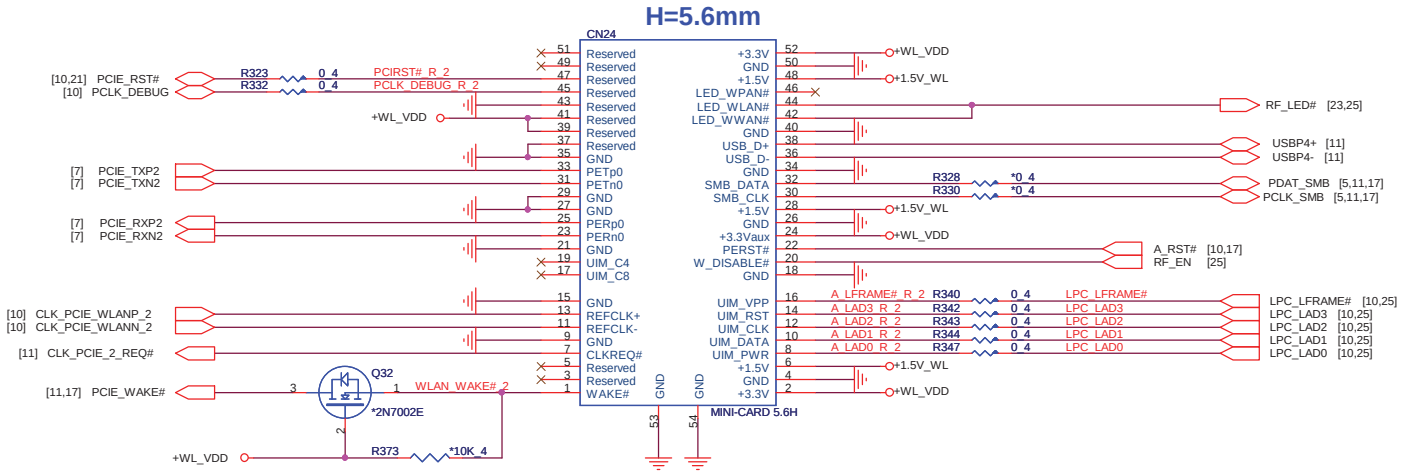
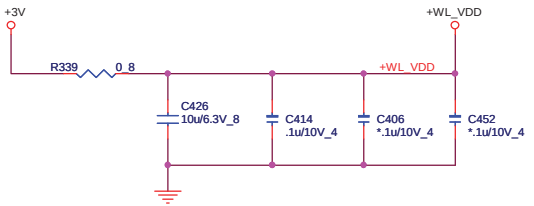
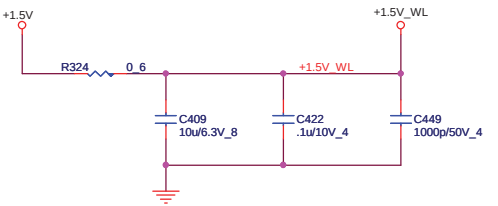
MINI-CARD WLAN(MNC)







PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	Mini-Card/WL	1A
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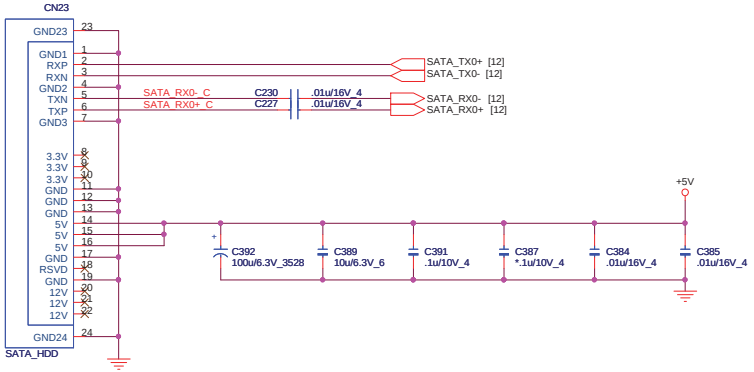
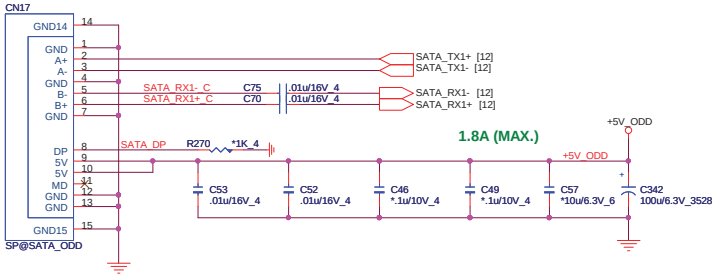
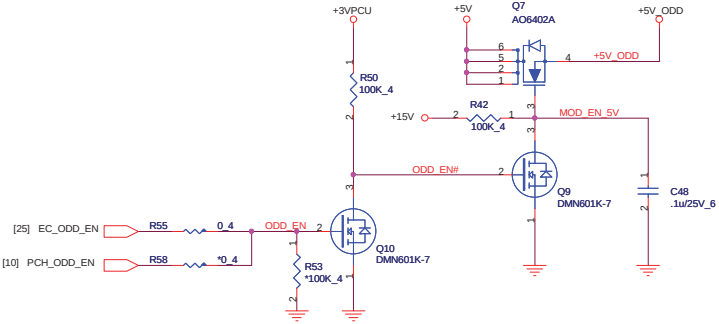
SATA HDD(HDD)



SATA ODD (ODD)



ODD POWER(ODD)



JM-9.5mm (H=2.4mm)/ Slim

Main	DFHS13FR078, DFHS13FR077
Second	DFHS13FR075

JV-12.7mm(H=5.5mm)/ Standard

Main	DFHS13FR017
Second	DFHS13FR006, DFHS13FR005

PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	SATA-HDD/ODD/HOLE	1A

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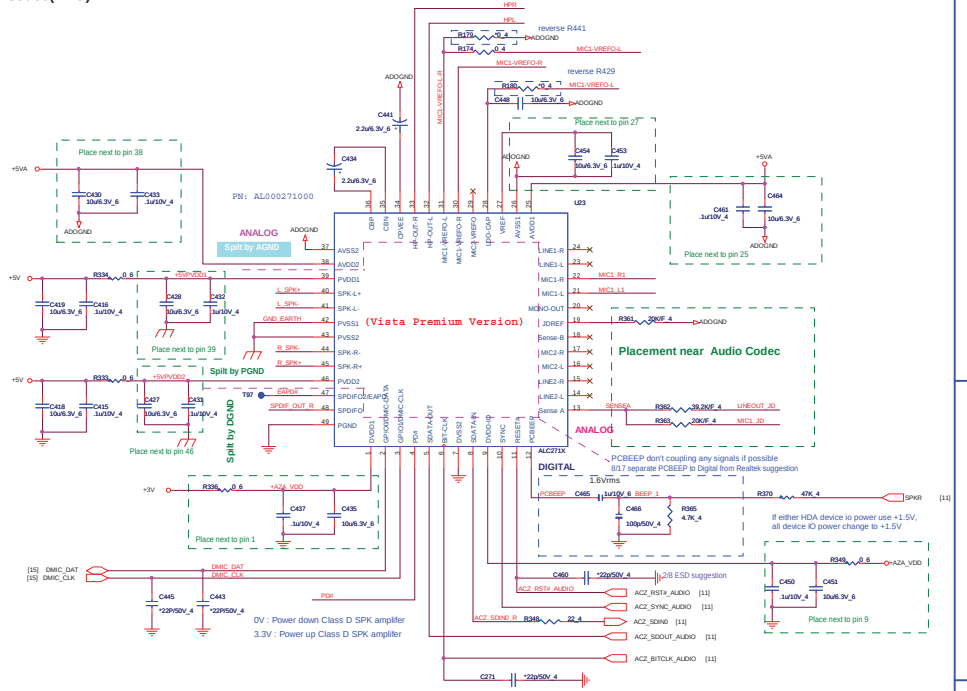
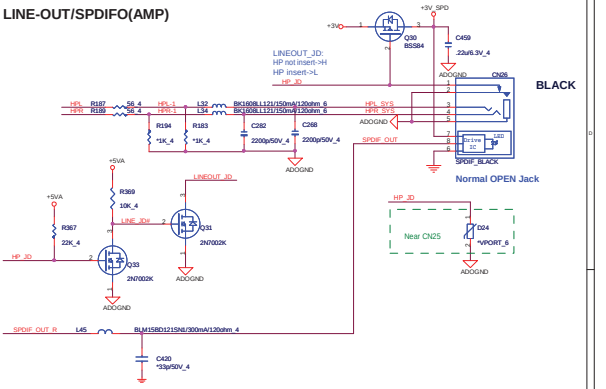
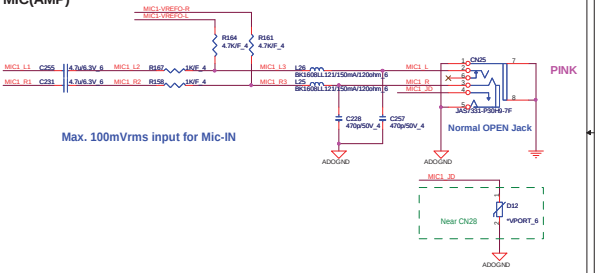
Codec(ADO)



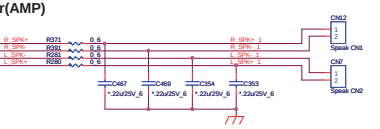
LINE-OUT/SPDIFO(AMP)



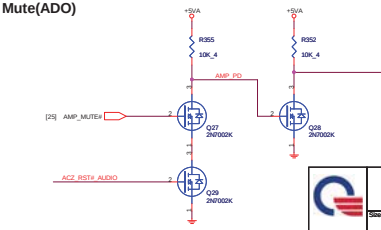
MIC(AMP)



Internal Speaker(AMP)



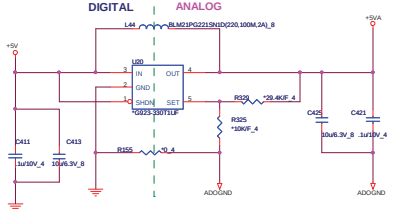
Mute(ADO)



Power (ADO)

Demodulation Filter

BEAD place close to CODEC.

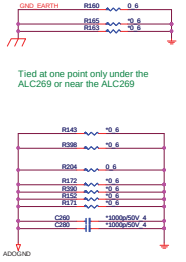


C656, C662 close U28 pin3 and L69

Vset =1.25V

Vout =Vset[1+AR(1,2)/AR(2,GND)]

GND_EARTH don't coupling AGND and SPK signals



Tied at one point only under the ALC269 or near the ALC269

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	ALC271X / AMP / SPK	1A

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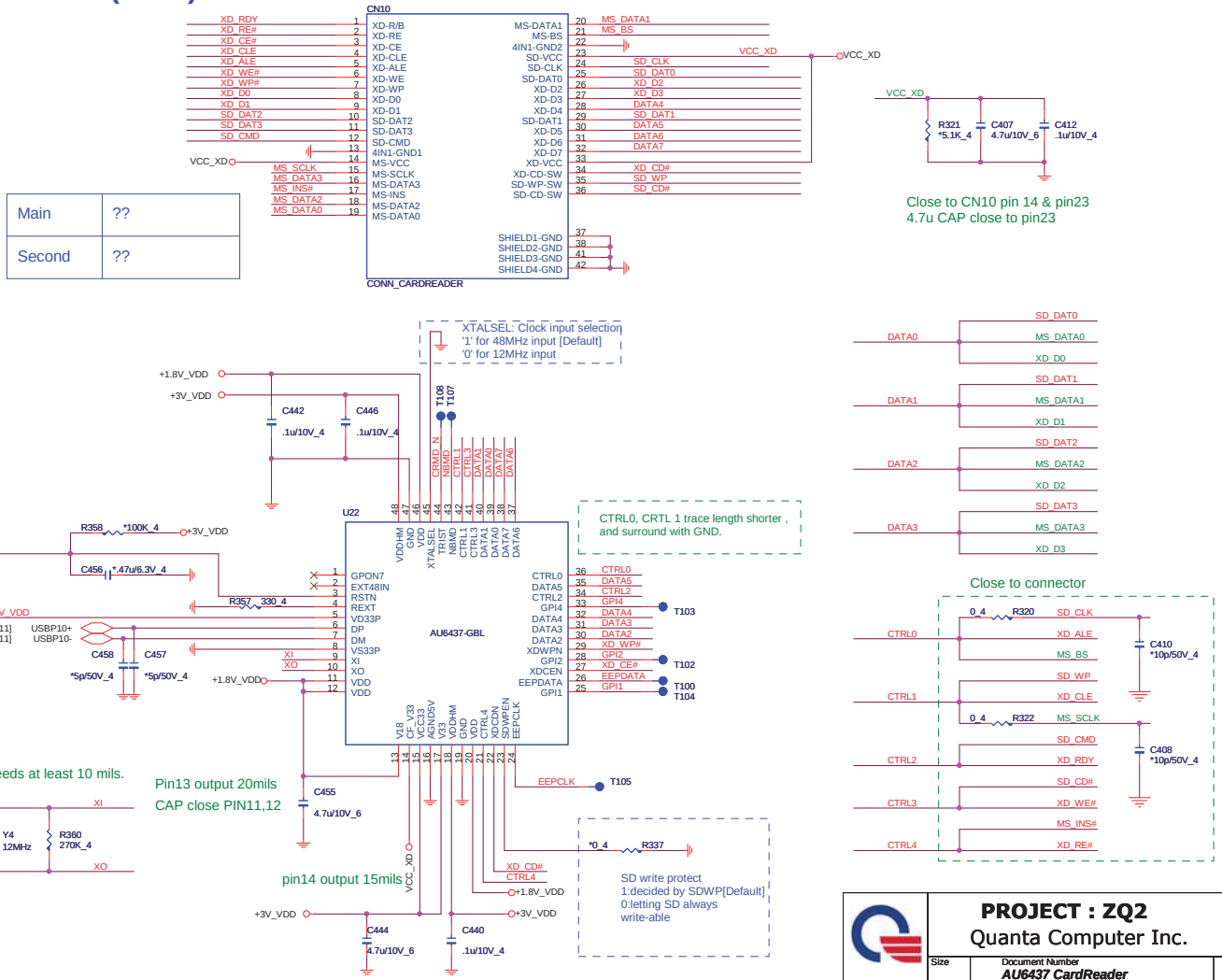
4 IN 1 CARD READER (MMC)



Size	Document Number: AU6437 CardReader
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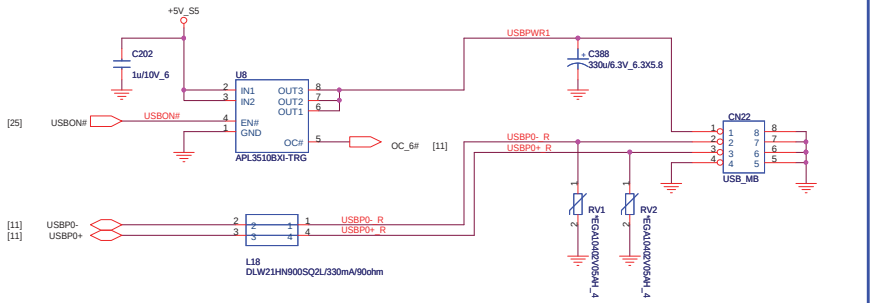
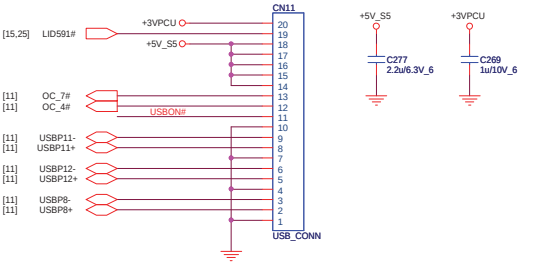
PROJECT : ZQ2

Quanta Computer Inc.

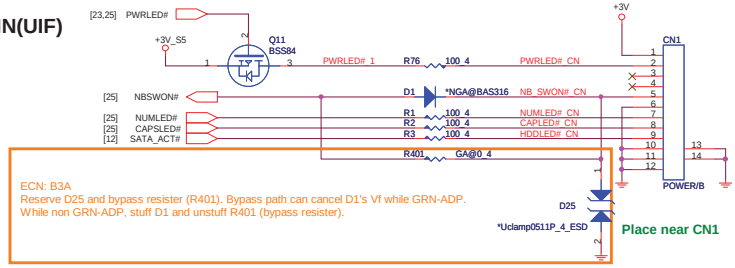
USB PORT(USB/MB)



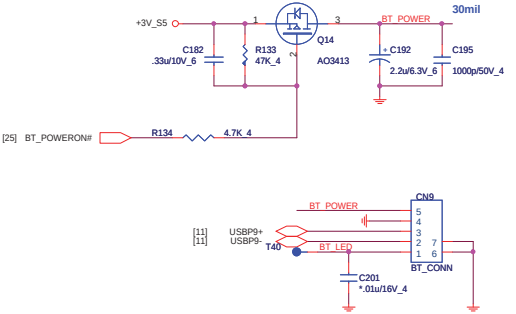
USB BOARD CONN(USB/SB)



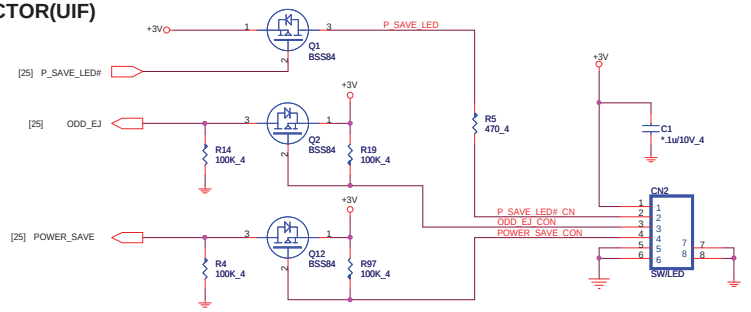
POWER BOARD CONN(UIF)



BLUETOOTH CONN(BTM)



LED BOARD CONNECTOR(UIF)



PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	USB/BT/TP	3A
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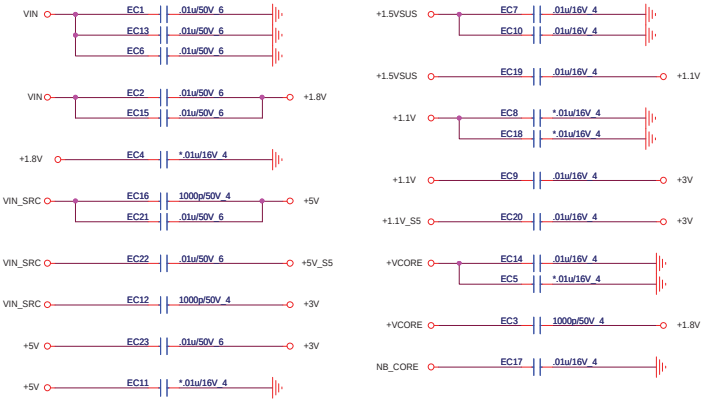
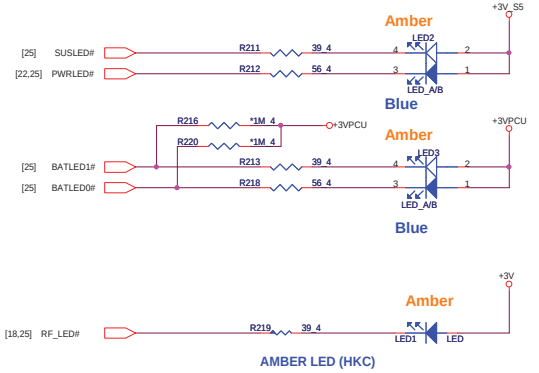
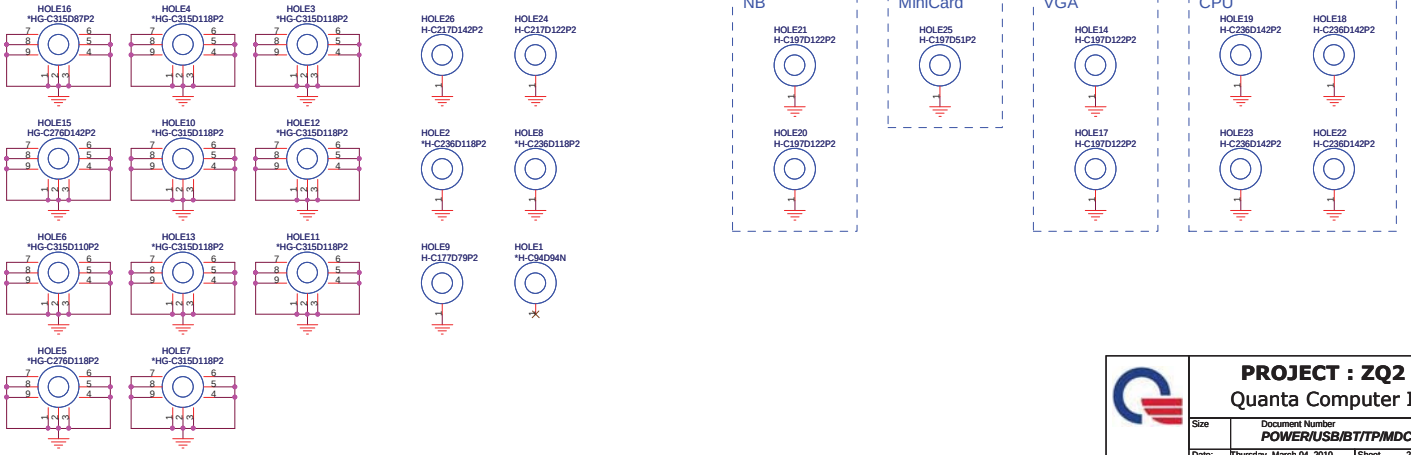
EE RETURN-PATH CAPACITORS(EMC)



LED(UIF)



HOLE(OTH)



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Quanta Computer Inc.

Size	Document Number	Rev
	POWER/USB/BT/TP/MDC	1A

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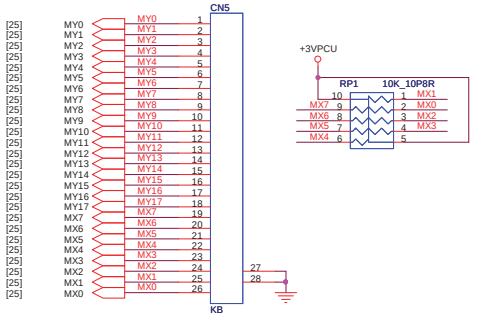
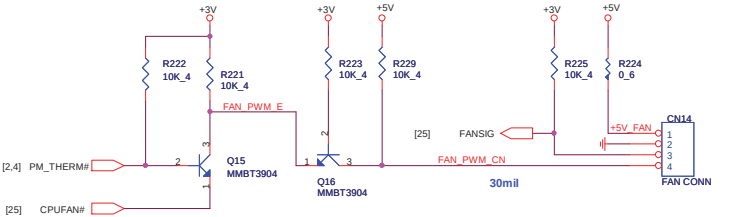
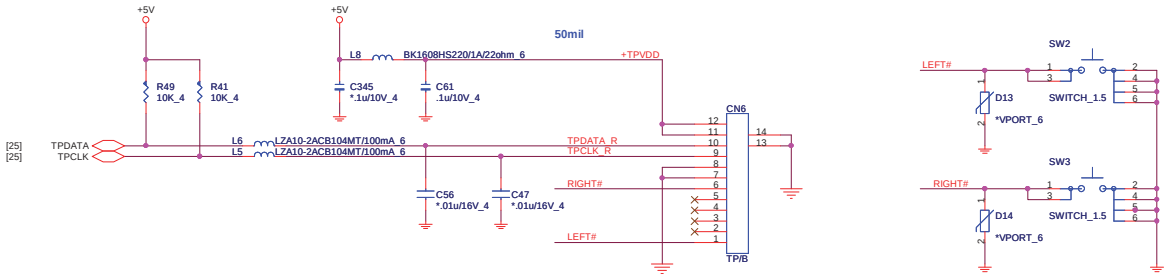
K/B(KBC)



CPU FAN(THM)



TOUCHPAD BOARD CONN(TPD)



PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	KB/FAN/EE RETURN CAP	1A

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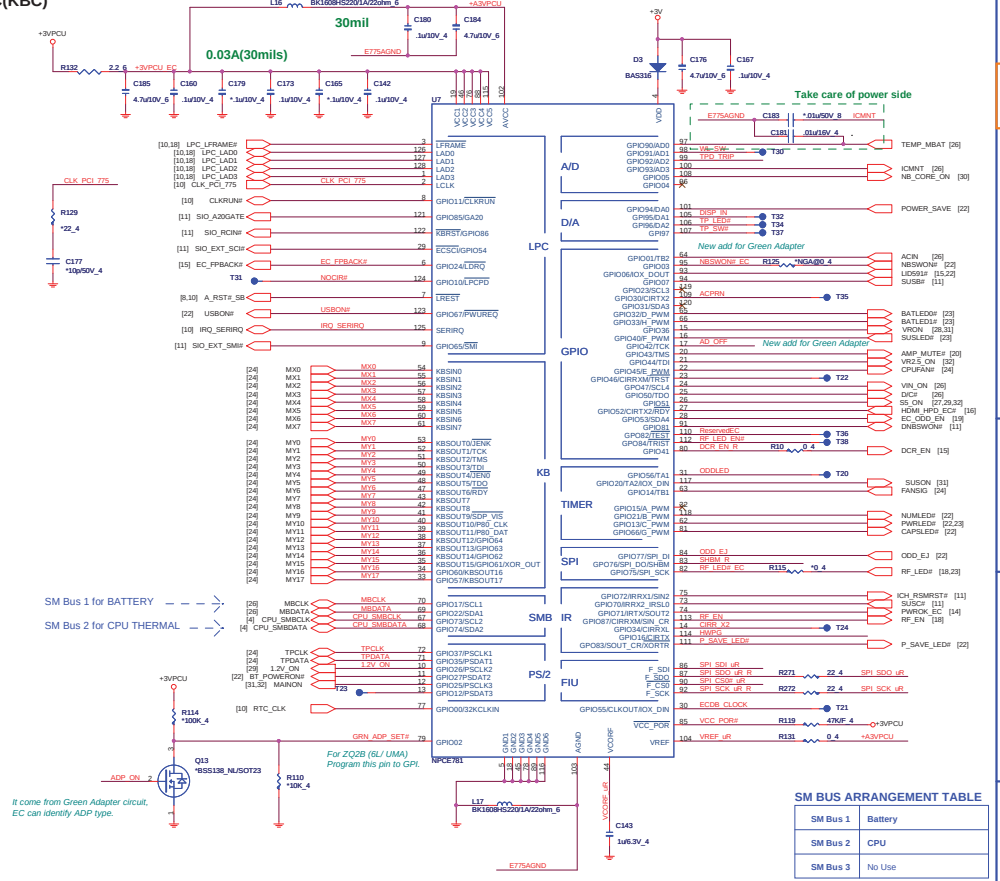
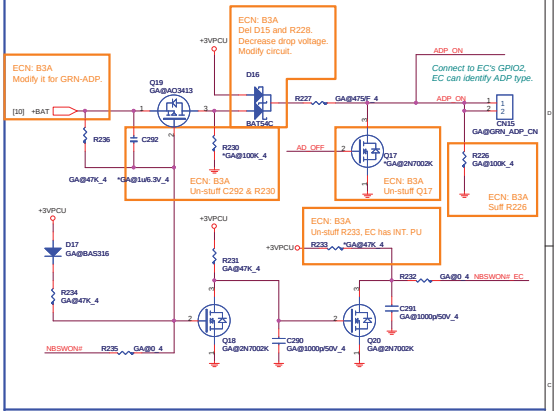
EC(KBC)



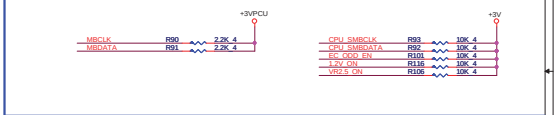
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	CPU
SM Bus 3	No Use

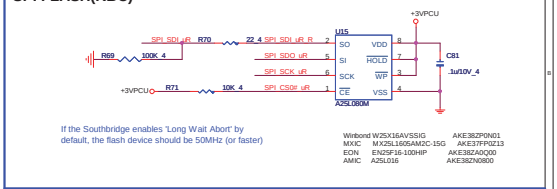
GREEN ADAPTER CIRCUIT



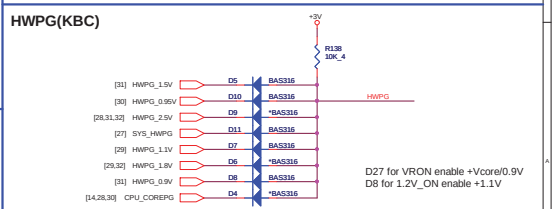
SM BUS PU(KBC)



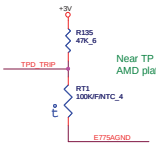
SPI FLASH(KBC)



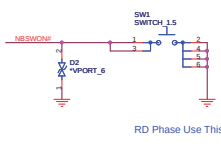
HWPG(KBC)



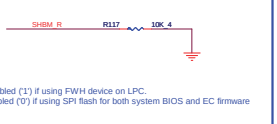
PALM REST THERMAL SENSOR (THM)



POWER-ON SWITCH (KBC)



POWER-ON SWITCH (KBC)



PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	3A

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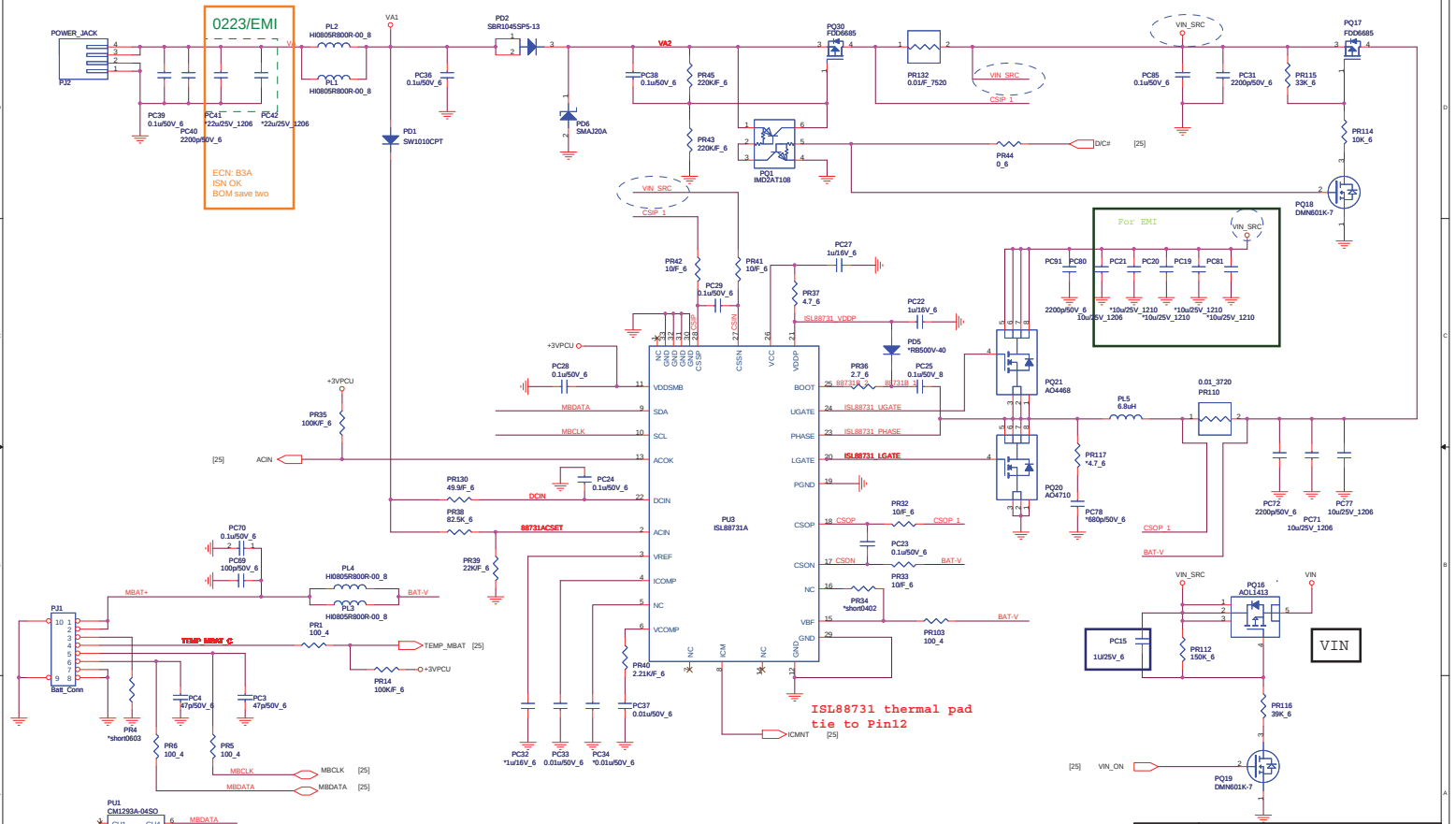
0223/EMI
ECN: B3A
ISN OK
BOM save two
POWER_JACK
PJ2
PL2
HI0805R800R-00_8
PL1
HI0805R800R-00_8
PC39
0.1u/50V_6
PC40
2200p/50V_6
PC41
22u/25V_1206
PC42
*22u/25V_1206
VA1
PD1
SW1010CPT
PC36
0.1u/50V_6
PD2
SBR1045SP5-13
PD6
SMAJ20A
VA2
PC38
0.1u/50V_6
PR45
220KF_6
PR43
220KF_6
PQ30
FDD6685
PR132
0.01/F_7520
VIN_SRC
CSIP_1
PQ1
IMD2AT108
PR44
0_6
D/C#
[25]
PC85
0.1u/50V_6
PC31
2200p/50V_6
PR115
33K_6
PQ17
FDD6685
PR114
10K_6
PQ18
DMN601K-7
For EMI
PC91
PC80
PC21
PC20
PC19
PC81
2200p/50V_6
10u/25V_1206
*10u/25V_1210
*10u/25V_1210
*10u/25V_1210
*10u/25V_1210
PR42
10/F_6
PR41
10/F_6
PC29
0.1u/50V_6
PC27
1u/16V_6
PR37
4.7_6
PC22
1u/16V_6
ISL88731_VDDP
PD5
*RB500V-40
PC25
0.1u/50V_8
PR36
2.7_6
88731A_3
88731B_3
+3VPCU
PC28
0.1u/50V_6
PR35
100KF_6
[25]
ACIN
MBDATA
MBCLK
PR130
49.9/F_6
DCIN
PC24
0.1u/50V_6
PR38
82.5K_6
88731ACSET
PR39
226/F_6
PC70
0.1u/50V_6
PC69
100p/50V_6
PL4
HI0805R800R-00_8
PL3
HI0805R800R-00_8
MBAT+
BAT-V
PJ1
Batt_Conn
TEMP_MBAT_C
PR1
100_4
TEMP_MBAT
[25]
PR14
100KF_6
+3VPCU
PR4
*short0603
PC4
47p/50V_6
PC3
47p/50V_6
PR6
100_4
PR5
100_4
MBCLK
MBDATA
PU1
CM1293A-04SO
CH1
CH4
VN
VP
CH2
CH3
TEMP_MBAT_C
PC43
22u/25V_6
Add ESD diode base on EC FAE suggestion
2/8: ESD suggestion
PU3
ISL88731A
NC
GND
GND
GND
GND
CSIP
CSIN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
ICM
NC
GND
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
CSOP
CSON
PR32
10/F_6
CSOP_1
PC23
0.1u/50V_6
BAT-V
PR33
10/F_6
PR34
*short0402
PR103
100_4
PR40
2.21KF_6
PC37
0.01u/50V_6
PC32
*1u/16V_6
PC33
0.01u/50V_6
PC34
*0.01u/50V_6
ICMNT
[25]
ISL88731 thermal pad
tie to Pin12
PQ21
AO4468
PQ20
AO4710
PL5
6.8uH
PR117
*4.7_6
PC78
*680p/50V_6
0.01_3720
PR110
PC72
2200p/50V_6
PC71
10u/25V_1206
PC77
10u/25V_1206
PQ16
AOL1413
VIN
PC15
1U/25V_6
PR112
150K_6
PR116
39K_6
[25]
VIN_ON
PQ19
DMN601K-7
PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number
CHARGER (ISL88731)
Rev
3A
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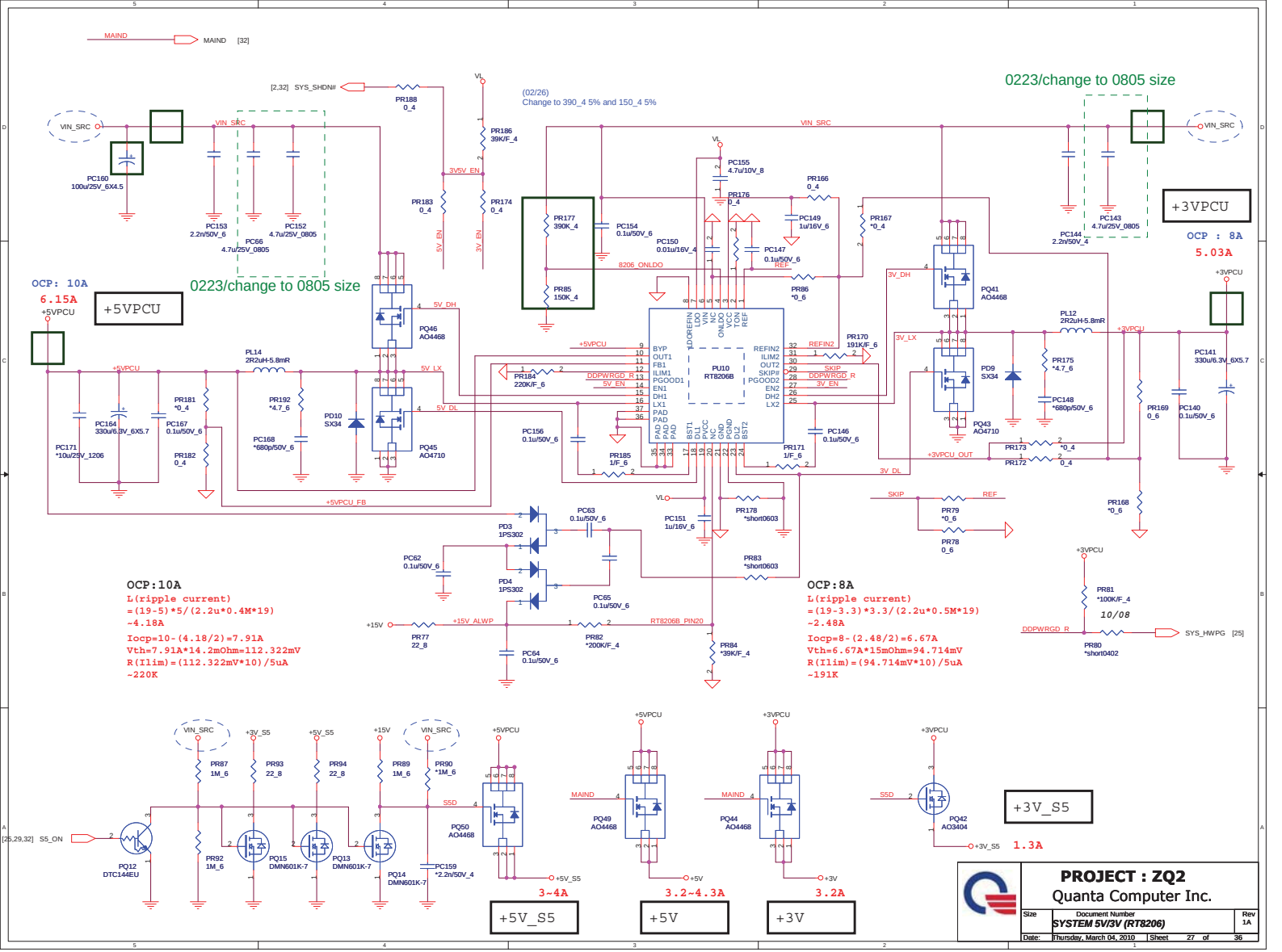
MAIND
MAIND [32]
[2,32] SYS_SHDN#
PR188 0_4
VL
PR186 39K/F_4
(02/26)
Change to 390_4 5% and 150_4 5%
0223/change to 0805 size
VIN_SRC
PC160 100u/25V_6X4.5
PC153 2.2n/50V_6
PC66 4.7u/25V_0805
PC152 4.7u/25V_0805
3V5V_EN
PR183 0_4
PR174 0_4
5V_EN
3V_EN
PR177 390K_4
PR85 150K_4
PC154 0.1u/50V_6
PC150 0.01u/16V_4
8206_ONLDO
PC155 4.7u/10V_8
PR176 0_4
PR166 0_4
PC149 1u/16V_6
PC147 0.1u/50V_6
REF
PR86 *0_6
PR167 *0_4
PC143 4.7u/25V_0805
PC144 2.2n/50V_4
+3VPCU
OCP : 8A
5.03A
OCP: 10A
6.15A
+5VPCU
+5VPCU
PR181 *0_4
PC164 330u/6.3V_6X5.7
PC167 0.1u/50V_6
PC171 *10u/25V_1206
PR182 0_4
PL14 2R2uH-5.8mR
PR192 *4.7_6
PD10 SX34
PC168 *680p/50V_6
5V_DH
5V_LX
5V_DL
PQ46 AO4468
PQ45 AO4710
+5VPCU_FB
PR184 220K/F_6
DDPWRGD_R
5V_EN
PU10 RT8206B
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
PAD
PAD
PAD
PAD
PAD
DORFIN
LDO
VIN
VCC
ONLDO
VCC
TON
OUT
REF
REFIN2
ILIM2
OUT2
SKIP2
PGOOD2
EN2
DH2
LX2
BST1
DL1
PVCC
GND
GND
PGND
DL2
SST2
REFIN2
SKIP
DDPWRGD_R
3V_EN
PR170 191K/F_6
PC156 0.1u/50V_6
PR185 1/F_6
PC146 0.1u/50V_6
PR171 1/F_6
3V_DH
3V_LX
3V_DL
PQ41 AO4468
PQ43 AO4710
PD9 SX34
PL12 2R2uH-5.8mR
PR175 *4.7_6
PC148 *680p/50V_6
PC141 330u/6.3V_6X5.7
PR169 0_6
PC140 0.1u/50V_6
PR173 *0_4
PR172 0_4
+3VPCU_OUT
PR168 *0_6
SKIP
REF
PR79 *0_6
PR78 0_6
PC63 0.1u/50V_6
PD3 1PS302
PD4 1PS302
PC62 0.1u/50V_6
PC65 0.1u/50V_6
PC151 1u/16V_6
PR178 *short0603
PR83 *short0603
+15V
+15V_ALWP
PR77 22_8
PR82 *200K/F_4
RT8206B_PIN20
PC64 0.1u/50V_6
PR84 *39K/F_4
PR81 *100K/F_4
10/08
DDPWRGD_R
PR80 *short0402
SYS_HWPG [25]
OCP:10A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=7.91A
Vth=7.91A*14.2mOhm=112.322mV
R(Ilim)=(112.322mV*10)/5uA
~220K
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K
VIN_SRC
+3V_S5
+5V_S5
+15V
VIN_SRC
+5VPCU
PR87 1M_6
PR93 22_8
PR94 22_8
PR89 1M_6
PR90 *1M_6
S5D
[25,29,32] S5_ON
PQ12 DTC144EU
PR92 1M_6
PQ15 DMN601K-7
PQ13 DMN601K-7
PQ14 DMN601K-7
PQ50 AO4468
PC159 *2.2n/50V_4
+5V_S5
3~4A
+5V_S5
+5VPCU
MAIND
PQ49 AO4468
+5V
3.2~4.3A
+5V
+3VPCU
MAIND
PQ44 AO4468
+3V
3.2A
+3V
+3VPCU
S5D
PQ42 AO3404
+3V_S5
1.3A
+3V_S5
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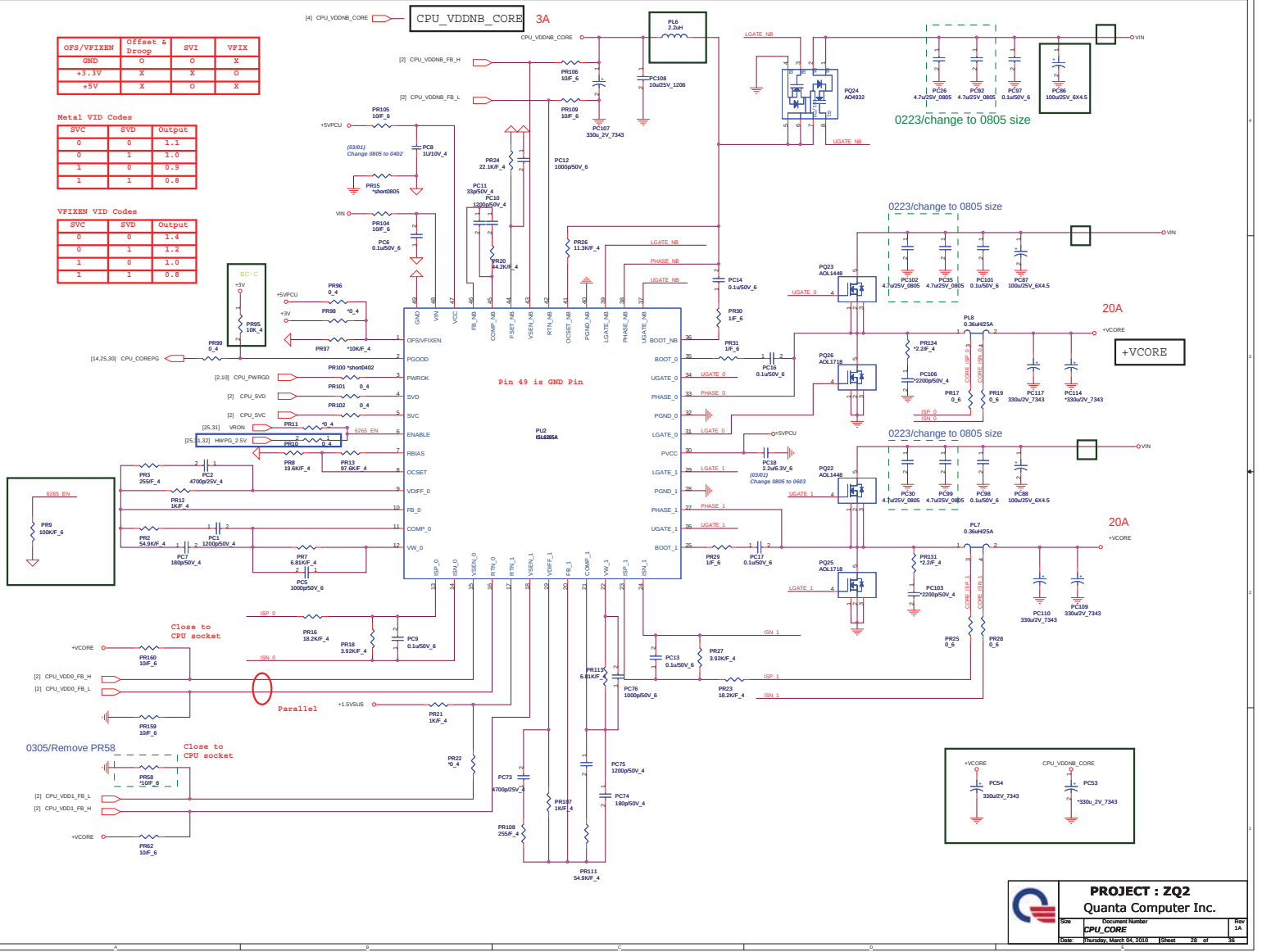
OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



Size	Document Number	Rev
	CPU_CORE	1A
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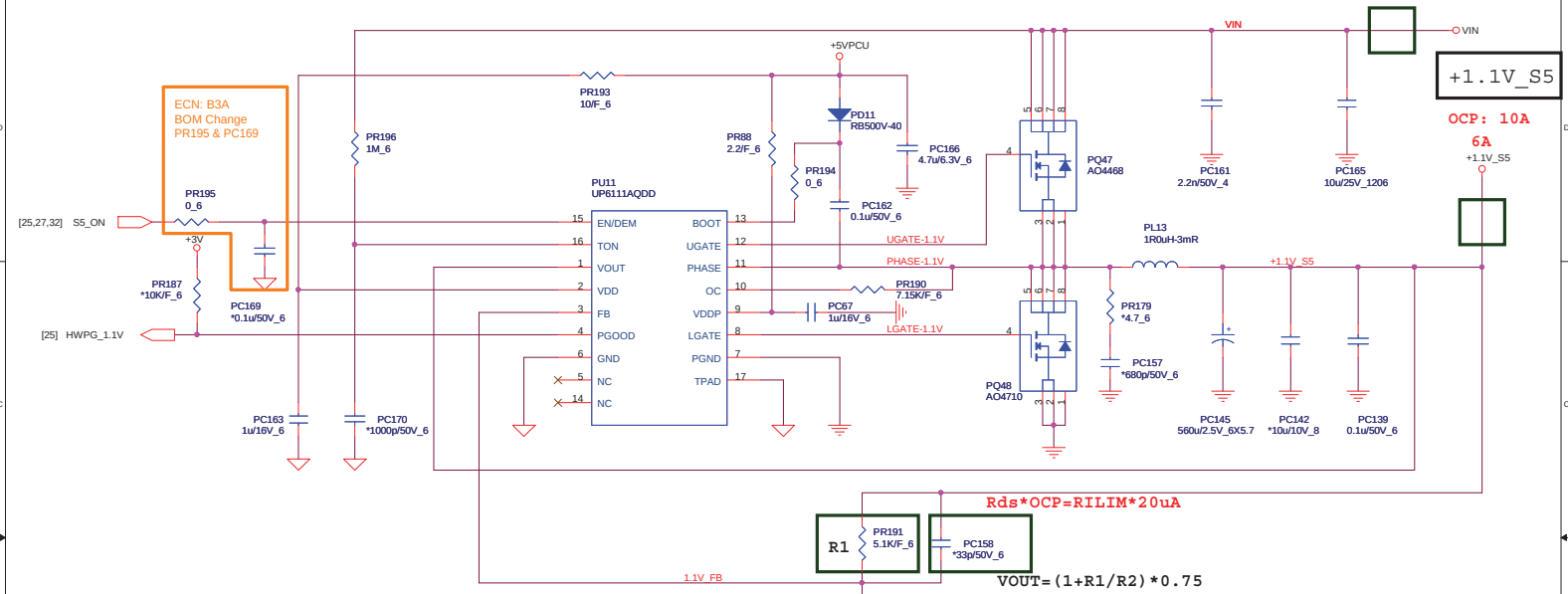


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

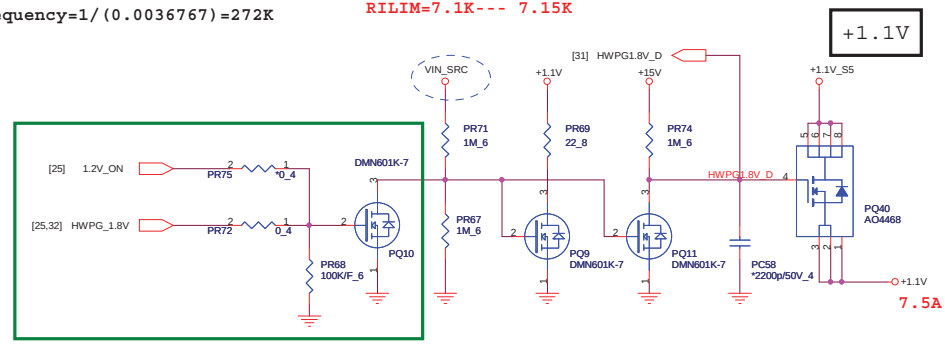
TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.1)*1.1/(1u*272k*19)
~3.81A

14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K



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	VCCP 1.1V(UP6111A)	3A
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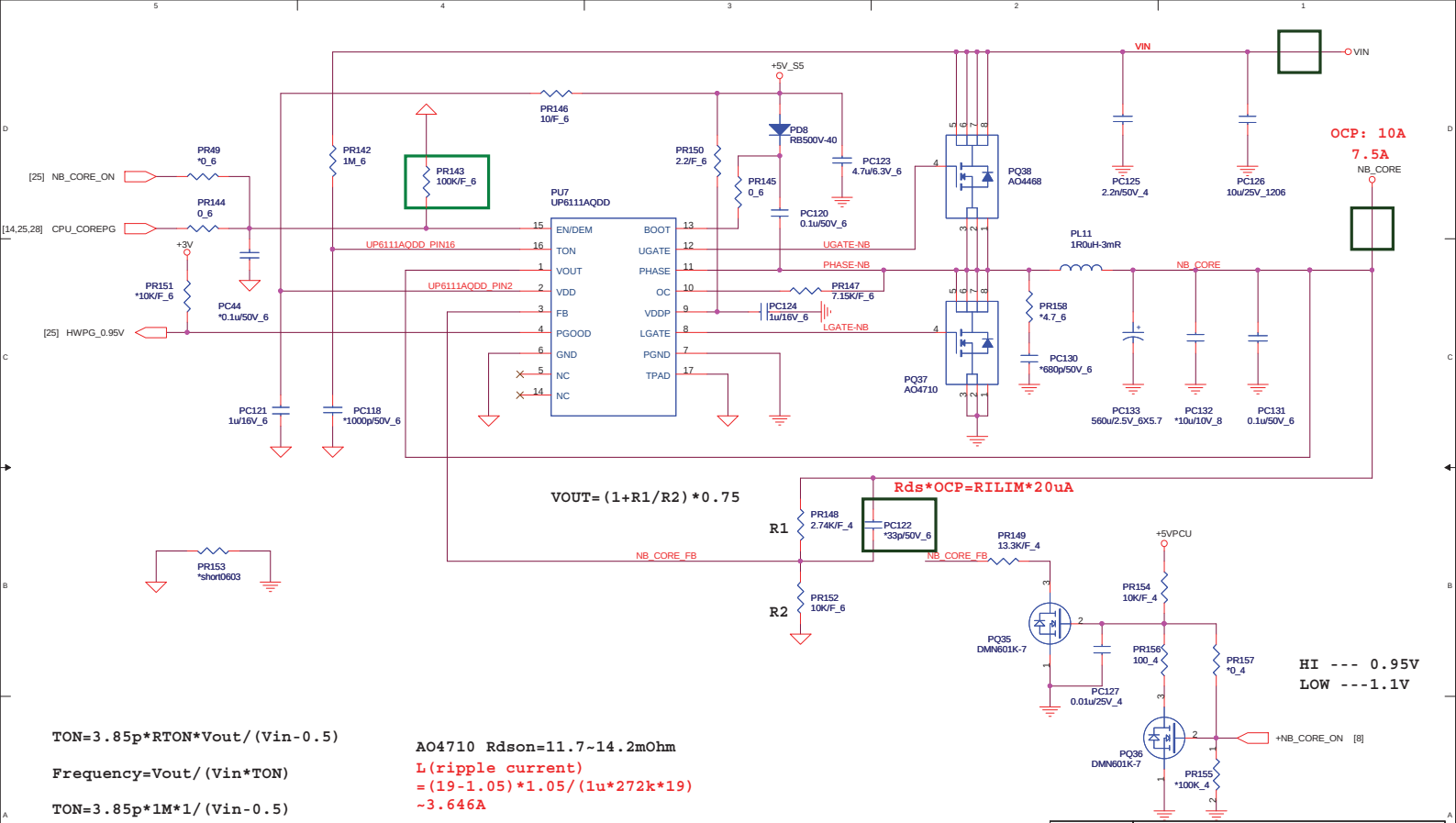

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K

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	NB_CORE(UP6111A)	1A
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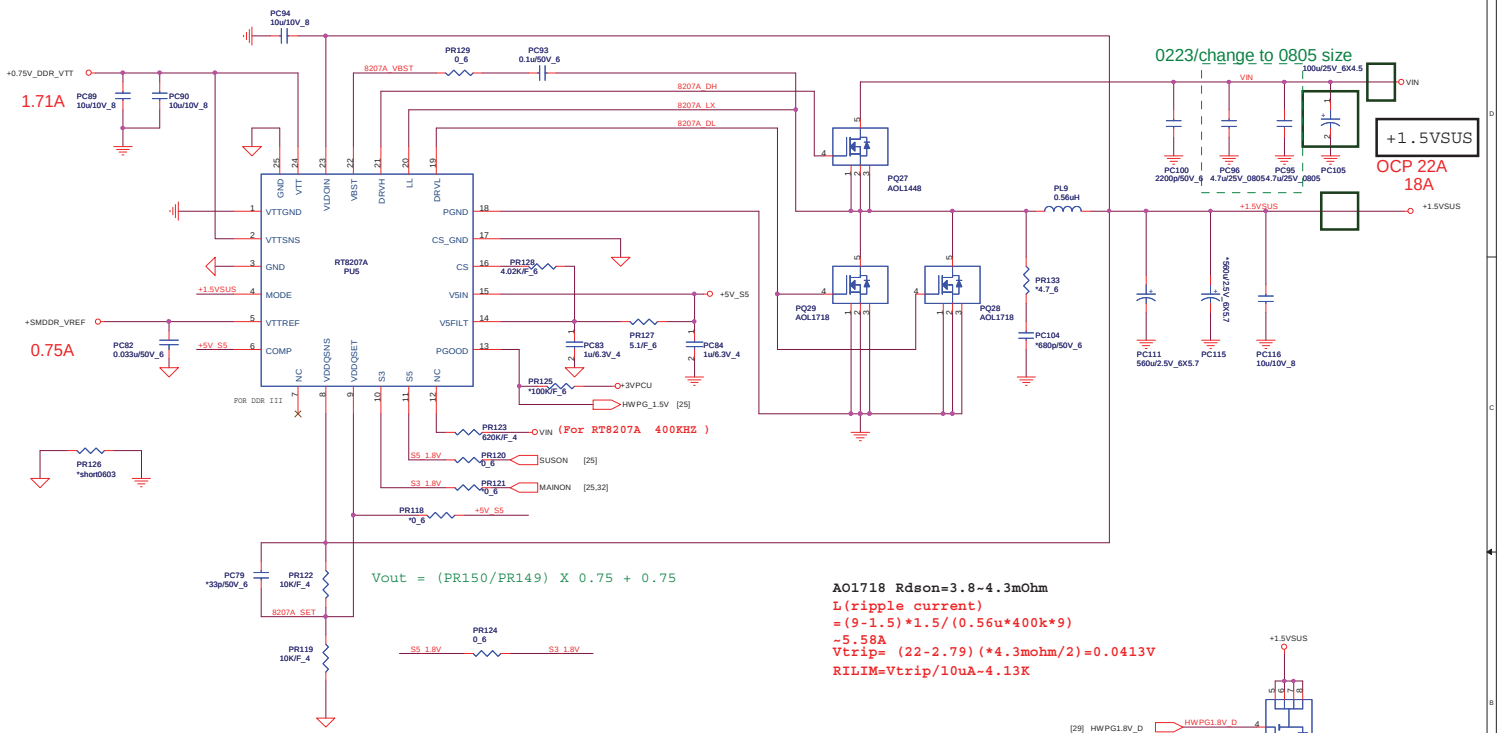
[PWM]



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	DDR 1.5V(TPS51116)	1A

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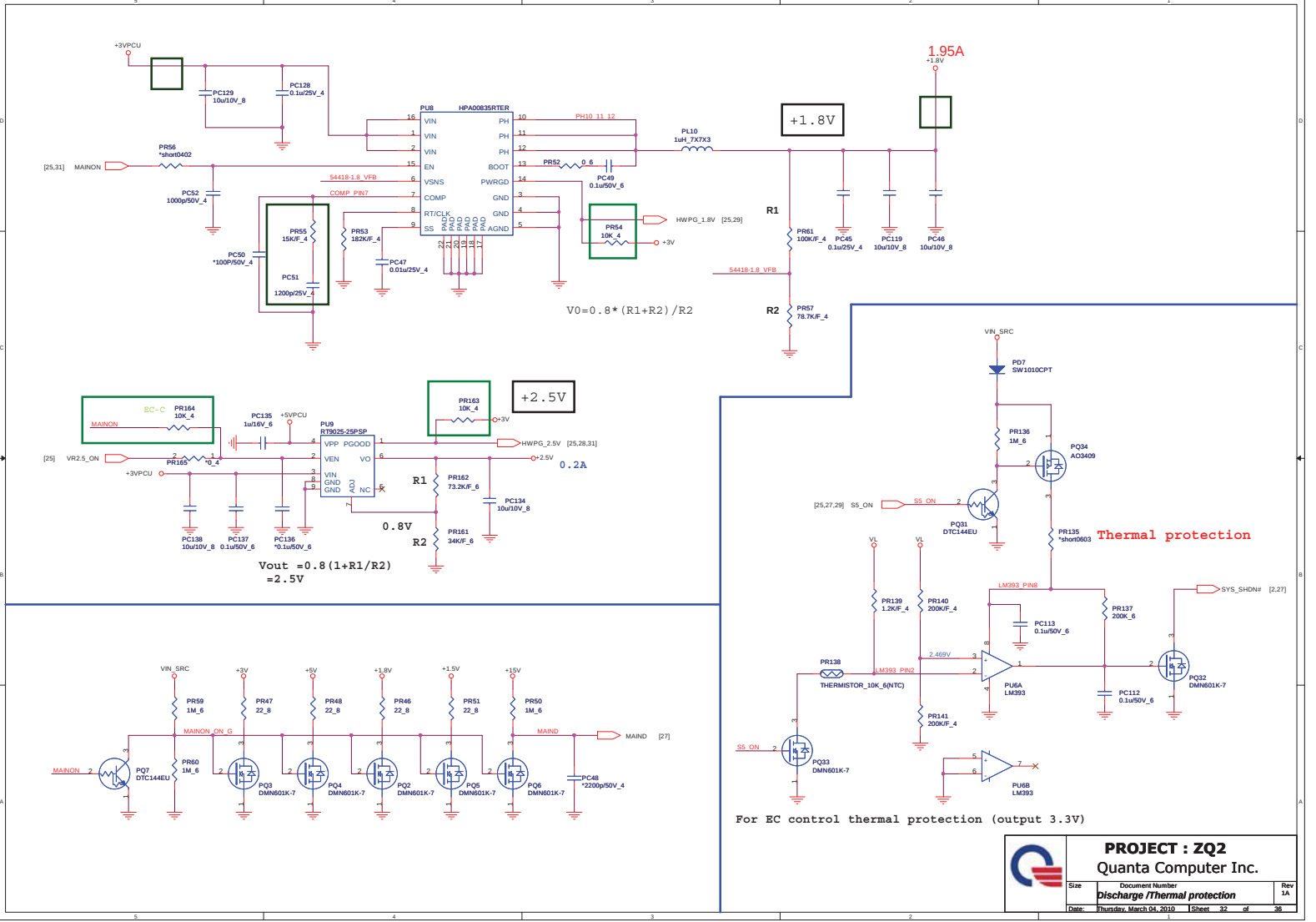

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	Discharge /Thermal protection	1A

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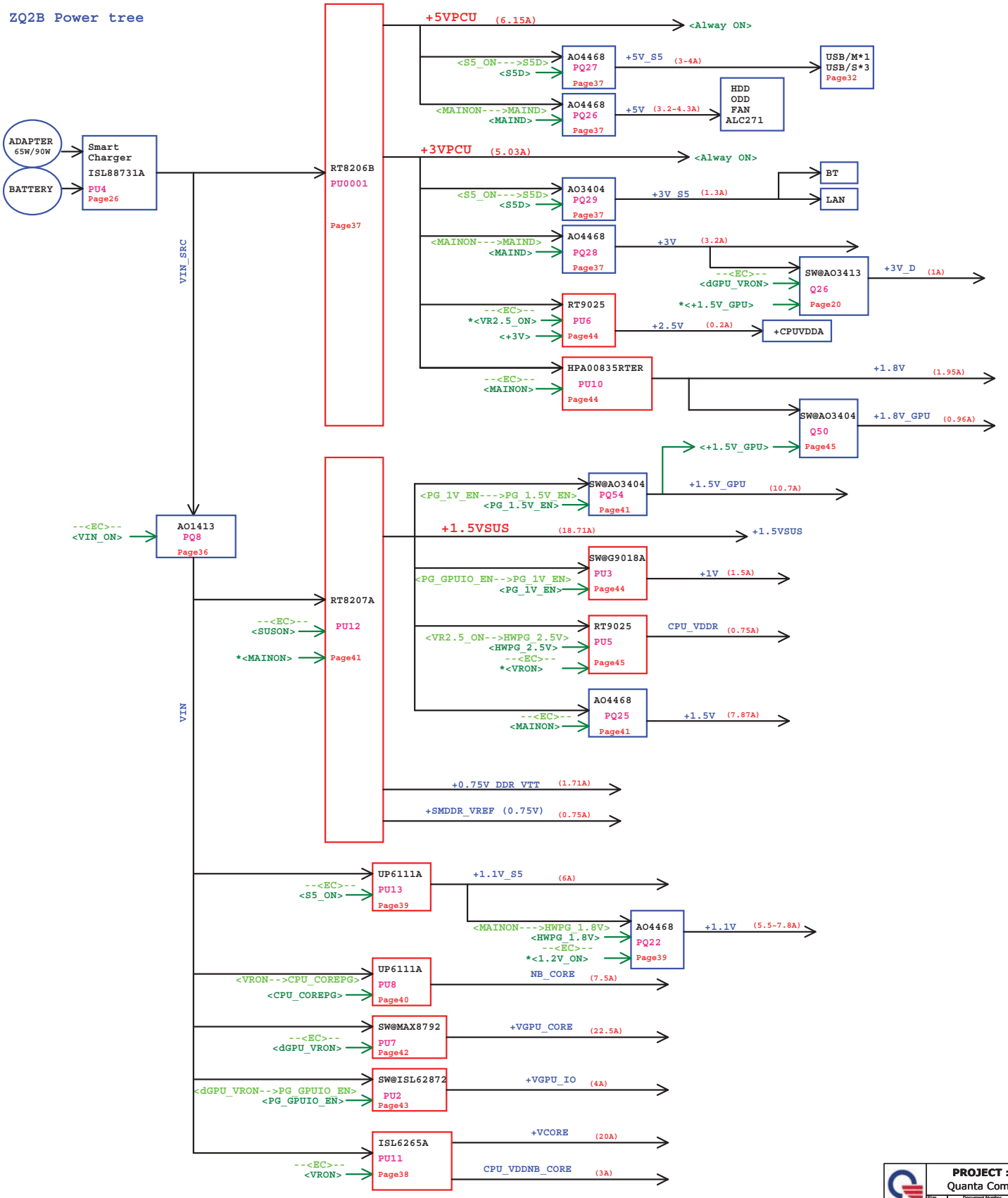
ZQ2B Power tree



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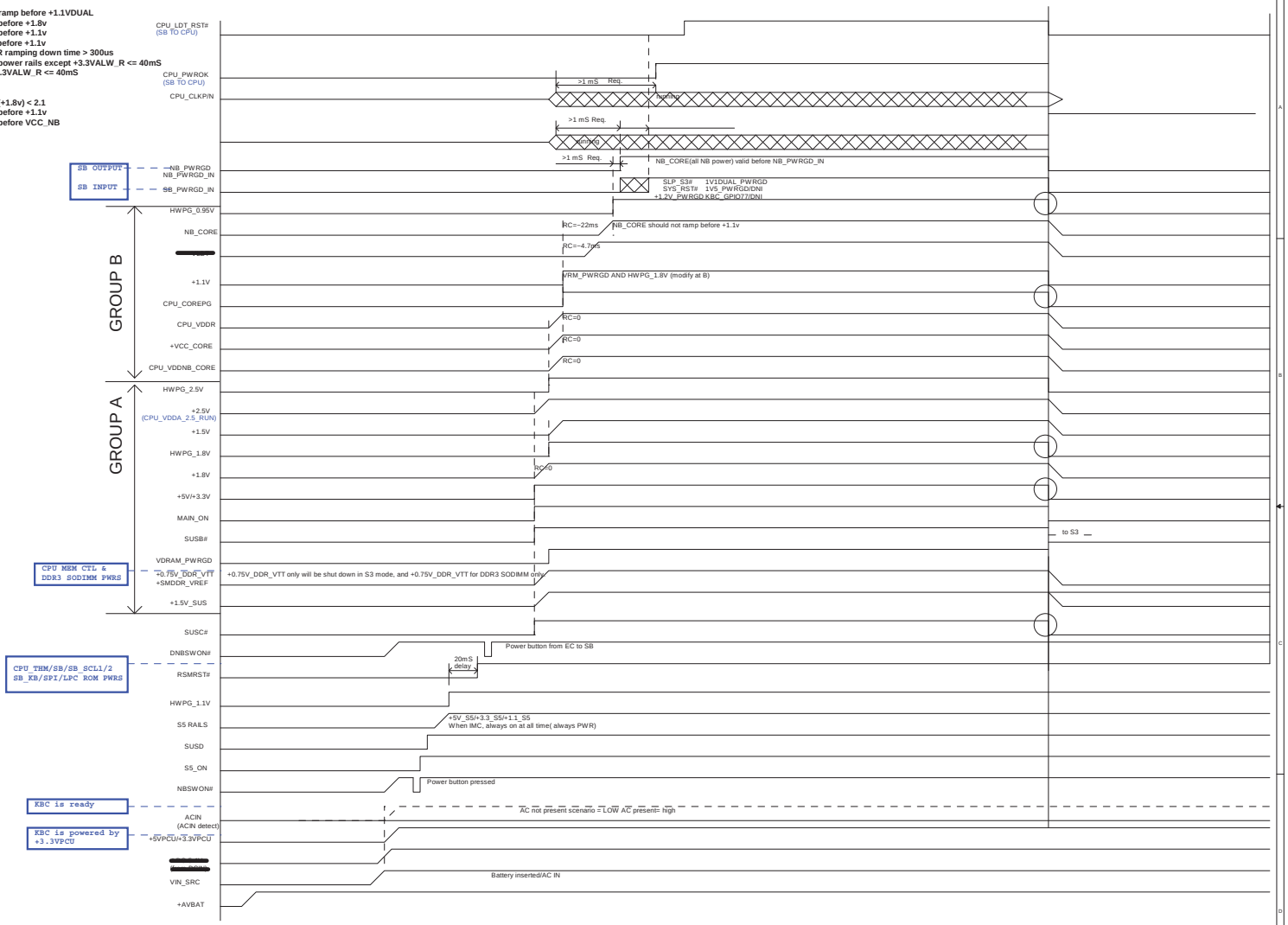
Power on Sequence required:

SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB



PROJECT : ZQ2 Quanta Computer Inc.		
Size	Document Number *Power Squence Chart*	Rev 1A
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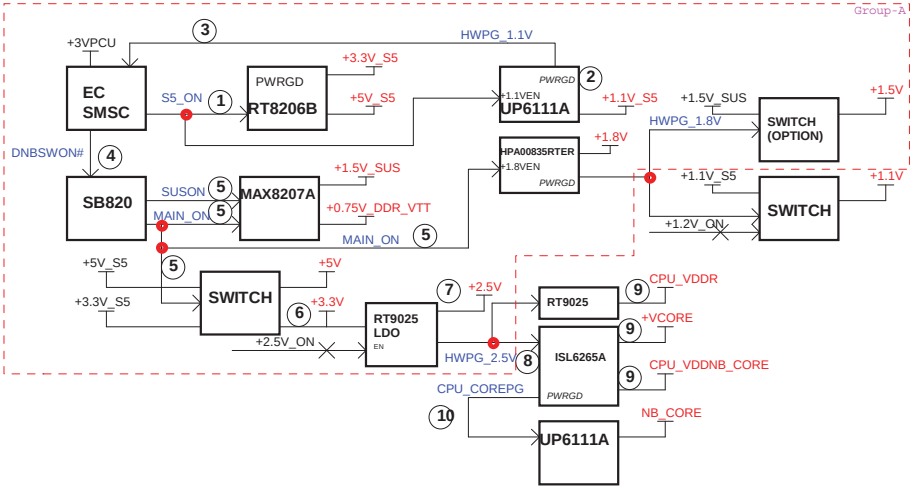


Power on Sequence required:

SB800:
1, +3.3V_S5 ramp before +1.1_S5
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB

POWER RAILS Sequencing

1	S5_ON	13	+1.8V	
2	+3.3V_S5	14	HWPG_1.8V	
3	+5V_S5	15	+1.5V	
4	+1.1V_S5	16	+2.5V	
5	HWPG_1.1V	17	HWPG_2.5V	
6	DNBSWON#	18	CPU_VDDNB_CORE	
7	SUSON	19	+VCC_CORE	
8	+1.5V_SUS	20	CPU_VDDR	
9	+SMDDR_VTERM	21	CPU_COREPG	
10	MAIN_ON	22	+1.1V	
11	+5V	23	NB_CORE	
12	+3.3V	24		

SB820 Sequencing

1	+3.3V_S5
2	ICH_RSMRST#
3	S0 POWER
4	PCIE_RCLKP/N
5	PCICLK[4:0]
6	SB_PWRGD_IN
7	NB_PWRGD_IN
8	LDT_PG
9	KBRST#
10	A_RST#
11	PCIRST#
12	LDT_RST#

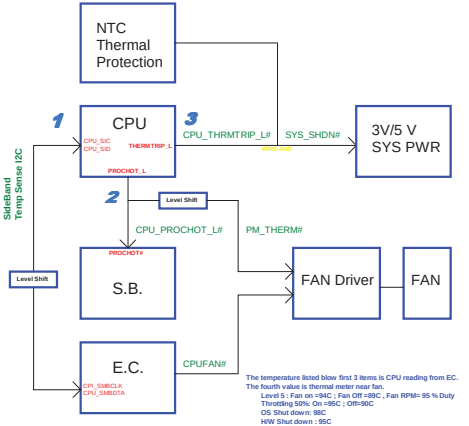
RS880 Sequencing

1	+3.3V
2	NB POWER RAILS
3	ATX PS_PWRGD
4	NB INPUT CLOCKS
5	CPUCLK
6	NB_PWRGD
7	SB_PWRGD
8	LDT_PG/CPU_PWRGD
9	PCIRST#,NB_RST#
10	LDT_RST#
11	
12	

EC Sequencing

1	3VPCU
2	NBSWON#
3	VIN_ON
4	S5_ON
5	ICH_RSMRST#
6	-DNBSWON#
7	SUSB#/SUSC#
8	SUSON/USB_ON#
9	MAIN_ON/HWPG
10	VRON
11	PWROK
12	

H/W Thermal Follow Chart



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Size	Document Number	Rev
	PWR ON SEQ and THERM POLICY	1A
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Model	REV	CHANGE LIST	MODEL	ZQ2B FROM	ZQ2B To
ZQ2B MB	1A	A1A The First Release.		X	1A
	3A	B3A Page 02 Q23 cahnge from FDV301V to BSS138. Becasue FDV301V EOL.		1A	3A
		B3A Page 10 Add off-page net of +BAT for Green Adpapter. It can decrease drop voltage. R289 change value to 12K beucase charge current.		1A	3A
		B3A Page 15 Change R11's footprint to short pad. BOM cancel R11.		1A	3A
		B3A Page 22 Reserve D25 and add R401. It can cancel D1's Vf while GRN-ADP.		1A	3A
		B3A Page 25 Del D15 and R228. And change PWR source of ADP_ON. All for decrease drop voltage. And un-stuff Q17 in oreder to EC suggestion.		1A	3A
		B3A Page 25 BOM change for fine-tune. Stuff R226 and BOM unstuff C292, R230 and R233.		1A	3A
		B3A Page 26 BOM save PC41 and PC42.		1A	3A
		B3A Page 29 BOM change for Pr195 and PC169 in order to AMD power up timing requirement.		1A	3A
				1A	
				1A	
				1A	
				1A	
				1A	
				1A	
				1A	
				1A	
				1A	
				1A	
				1A	
				1A	
				1A	
				1A	
				1A	
				1A	

DOC NO.	PROJECT MODEL :	ZQ2B	APPROVED BY:		DATE:	2010/03/05
	PART NUMBER:		DRAWING BY:		REVISON:	1A

PROJECT : ZQ2

Quanta Computer Inc.

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	Change list	1A

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